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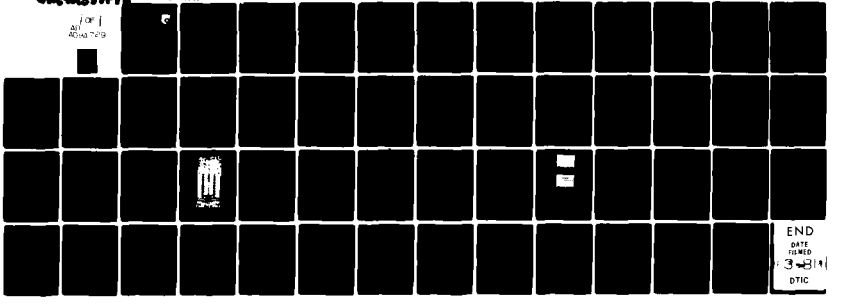

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DESIGN OF A LOW-POWER SCHOTTKY TTL HIGH-SPEED DIGITAL PHASE-LOCKED LOOP INTEGRATED CIRCUIT

Texas Instruments Incorporated
P.O. Box 225012
Dallas, Texas 75265

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October 1980

Technical Report AFWAL-TR-80-1152
Final Report for Period April 1977 – June 1980

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Design & Packaging Group

GARY K. PRITHCARD, Lt Col, USAF
Chief, Design & Packaging Group
Microelectronics Branch

FOR THE COMMANDER

STANLEY E. WAGNER, Chief
Microelectronics Branch
Electronic Technology Division

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A high speed digital phase-locked loop (DPLL) integrated circuit was successfully designed and implemented with Low Power Schottky technology. The Avionics Laboratory sponsored the development of the SN54LS297 DPLL IC, which was designed to become a standard Texas Instruments catalog part. This device uses strictly digital techniques to perform the first order phase-locked loop linear function and can be cascaded to form higher order phase filters. The center frequency and bandwidth are digitally programmable, and Q's of 8 to 130,000 can be obtained, making possible narrow-bandwidth phase tracking with higher resolution than conventional phase-locked loops.

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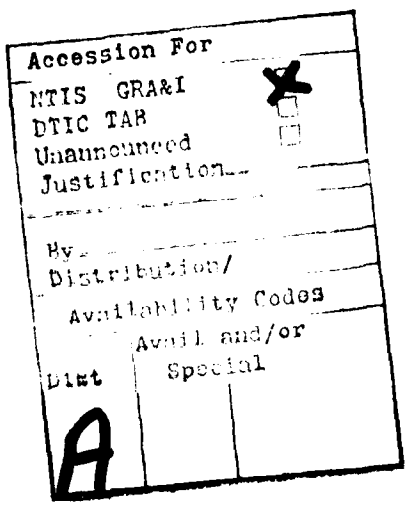
FOREWORD

This Final Report describes the work performed by Texas Instruments Incorporated, Semiconductor Group, Dallas, Texas, under Contract No. F33615-77-C-1047 from April 1977 to June 1980. The Air Force program monitor is W. B. Williams (AFWAL/AADE-3).

This program was administered by the Military Products department of Texas Instruments. Project research was jointly directed by the Military Products department and the Low Power Schottky department in order to fully enhance both the military and the commercial market potential of the Digital Phase-Locked Loop Integrated Circuit. The Military Products Strategic Marketing Manager is Wayne Howse, and the Low Power Schottky Operations Manager is W.T. Greer.

The initial integrated circuit design was begun at Texas Instruments by Thurman Dobbs under the Air Force technical supervision of Gary Gaugler. In March 1978, the design responsibility was transferred to James Gallia. Cory Dooley assisted in the research. Project technical management was carried out by Hugh Johnson and Vern Hardin. This report was submitted to the AFWAL for approval on July 31, 1980.



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SECTION I
INTRODUCTION

Present methods of system designers for phase and frequency processing include active and passive filters, analog phase-locked loops and computer-based algorithms. This report discusses the implementation of the digital phase-locked loop integrated circuit which has significant advantages in performance compared to the above conventional methods.

Recent trends towards all digital signal processing and digital control of signal processing systems greatly increase the complexity of systems utilizing analog components. Active and passive filters must be specifically designed for each application and their performance can be impacted by environmental conditions. Narrow bandwidth filters are difficult and expensive to design, especially when variable bandwidth is required. Analog-to-digital conversion must be applied to the phase information of the processed signals. While readily adaptable to many systems, analog phase-locked loop integrated circuits are susceptible to performance deterioration due to variations of voltage, temperature or external components. Because of this, their ability to provide high-resolution narrow-bandwidth systems is limited. Computer simulation of high performance phase-locked loops can be used to achieve narrow-bandwidth processing, but the cost or system size of this approach may be unacceptable in many applications.

The digital phase-locked loop (DPLL) performs the first-order phase-locked loop linear function using no analog components. The accuracy of the circuit is dependent only on the system clock, not on supply voltage or temperature. The center frequency and bandwidth are digitally programmable, and Q's of 8 to 130,000 can be obtained, making possible narrow-bandwidth phase tracking with higher phase resolution than conventional phase-locked loops.

The objective of this program is to integrate the DPLL system on a single chip, utilizing Low Power Schottky technology. For maximum marketability to both commercial and military products, this integrated DPLL will be capable of high-speed operation while keeping power dissipation to a reliable limit. The circuit is to be fully TTL compatible and capable of qualification to military standard MIL-M-38510.

SECTION II
SCOPE

This effort is to develop, fabricate and test an integrated digital phase-locked loop (DPLL) using Texas Instruments TTL Low Power Schottky technology. A quantity of 50 tested DPLL devices in ceramic packages and 50 tested devices in plastic packages will be delivered to the AFAL for evaluation. The integrated circuit will be developed to be suitable for both military and commercial systems, with the objective that the DPLL device become a standard Low Power Schottky catalog item, designated the SN54/74LS297.

SECTION III
DIGITAL PHASE-LOCKED LOOP OPERATION

A. OVERVIEW

The block diagram of Figure 1 shows the four main segments of a digital phase-locked loop (DPLL) system[1,2] as they would be connected for a typical application. The phase detector compares the phase of the input signal ϕ_{IN} with the phase of the output signal ϕ_{OUT}. The phase detector output is a phase error signal that is digitally integrated by the K-counter circuit of variable modulus K. The carry (CA) and borrow (BO) outputs of the K-counter control the Increment/Decrement (I/D) circuit. The I/D circuit adds or deletes pulses from the input clock signal which is a multiple 2N of the loop center frequency f_c. The I/D output then is an altered clock signal with added or deleted pulses according to the phase error signal of the phase detector. The I/D output is filtered by the external ÷N counter to provide ϕ_{OUT}, which inputs the phase detector to complete the loop. As long as the input signal frequency f_{IN} is within a prescribed Δf of f_c, i.e., within the lock range of the DPLL, the frequency of the output signal f_{OUT} will equal f_{IN} and a definite phase error will exist between the two signals. Changing the counter modulus K controls the degree of phase error and the loop bandwidth.

B. PHASE DETECTORS

The phase detector generates an error signal waveform which at zero phase error is a 50% duty cycle square wave. At the limits of linear operation, the phase detector output will be either high or low all of the time, depending on the direction of the phase error (ϕ_{IN} ϕ_{OUT}). Within these limits, the phase detector output varies linearly with the input phase error according to the gain K_D which is expressed in terms of phase detector output per cycle of phase error. The phase detector output can be defined to vary between ±1 according to the relation:

$$PD_{OUT} = \frac{\%\ HIGH \quad \%\ LOW}{100} \qquad (1)$$

The output of the phase detector will be $K_D \phi_E$, where the phase error, $\phi_E = \phi_{IN}$ ϕ_{OUT}.

Exclusive-OR phase detectors (EXORPD) and Edge Controlled phase detectors (ECPD) are commonly used digital types. The ECPD is more complex than the EXORPD logic function, but can be described generally as a circuit that changes states on the negative transitions of its inputs. K_D for an EXORPD is 4 because its output is high ($PD_{OUT} = 1$) for a phase error of 1/4 cycle. Similarly, K_D for the ECPD is 2 since its output is high for a phase error of 1/2 cycle. The type of phase detector will determine the zero phase error point, i.e., the phase separation of the phase detector inputs for ϕ_E defined to be zero. For the basic DPLL system of Figure 1, $\phi_E = 0$ when the phase detector output is a square wave. The EXORPD inputs are 1/4 cycle out of phase for zero phase error. For the ECPD, $\phi_E = 0$ when the inputs are 1/2 cycle out of phase.

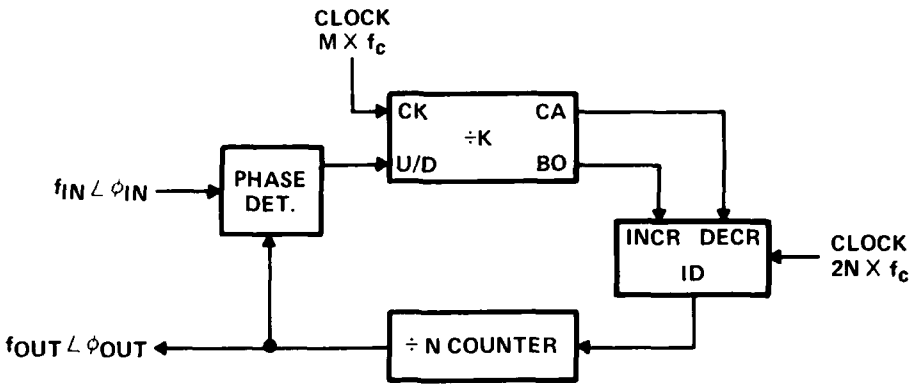


Figure 1. Basic Digital Phase-Locked Loop Block Diagram

C. K-COUNTER AND INCREMENT/DECREMENT FUNCTION

The output of the phase detector feeds the Up/Down (U/D) input of the K-counter. The K-counter may be implemented in numerous ways, but for the sake of discussion, it is best thought of as an up/down counter of modulus K with an input clock of M times the center frequency (f_c) of the loop. The K-counter counts up or down depending on the level of the PD output and thereby performs a digital integration of the PD output over a period of time determined by the K-counter clock. The average count contained in the K-counter will change with time and eventually recirculate and generate a carry (CA) pulse if recirculation occurs while counting up, or a borrow pulse if recirculation occurs while counting down. The K-counter can be considered a frequency divider with a ratio Mf_c/K. If the carry output pulses are considered positive pulses and the borrow output pulses considered negative pulses, then the combined K-counter output can be defined as:

$$K_{OUT} = \frac{K_D \phi_E M f_c}{K} \quad H_Z \tag{2}$$

The K-counter outputs drive the increment and decrement inputs of the I/D circuit. The third input to the I/D circuit is a clock having a frequency 2N times f_c where N is the modulus of the ÷N external feedback counter. When there are no input pulses from the K-counter, the I/D circuit output will be one-half the input clock frequency. Each time the I/D circuit receives a pulse on the INCR or DECR inputs, it adds or deletes 1/2 cycle from the ÷2 output waveform, I/D_{OUT}. The output of the I/D circuit can be expressed:

$$I/D_{OUT} = Nf_c + \frac{K_D \phi_E M f_c}{2K} \quad H_Z \tag{3}$$

D. DPLL LOCK EQUATIONS

The MSB output of the ÷N counter provides the loop output:

$$f_{OUT} = f_c + \frac{K_D M f_c \phi_E}{2KN} \quad H_Z \tag{4}$$

The range of frequency tracking, Δf_{max}, can be determined from the above equation since the phase detector output $K_D \phi_E$ equals 1 at the edge of the lock range:

$$\Delta f_{max} = f_{OUT\ max} - f_c = \frac{Mf_c}{2KN} \quad Hz \tag{5}$$

Within the lock range ($f_c \pm \Delta f_{max}$), f_{OUT} equals f_{IN} and the phase error vs input frequency deviation is given by:

$$\phi_E = \frac{2KN}{K_D M f_c} (f_{IN} - f_c) \quad cycles \tag{6}$$

where

$$\phi_E = 0 \text{ for } f_{IN} = f_c$$

These results correspond to a similar relationship for the output in hertz of a first order analog phase-locked loop:[3]

$$f_{OUT} = f_c + (K_V K_D)\phi_E \quad Hz \tag{7}$$

where the phase detector output $K_D \phi_E$ is in volts, and the voltage controlled oscillator has a center frequency f_c and a gain K_V in hertz/volt.

The bandwidth of a DPLL can be determined from the open-loop transfer function.[1] The 3-dB frequency is given by:

$$\omega_{3dB} = \frac{K_D M f_c}{2KN} \quad radians/sec \tag{8}$$

The parameter Q of a PLL relates the bandwidth, $\omega_{3\ dB}$, to ω_c, the loop center frequency in radians. The Q of the DPLL is given by:

$$Q = \frac{\omega_c}{2\omega_{3dB}} = \frac{2\pi f_c}{\frac{K_D M f_c}{KN}} = \frac{\pi K}{K_D} \tag{9}$$

where both the K clock input and the I/D clock input receive the same input clock frequency (M=2N).

E. RIPPLE CANCELLATION

The phase tracking resolution of the DPLL depends on the modulus of the ÷N counter. Each increment or decrement operation by the I/D circuit corrects the phase of the ÷N counter input by 1/2 cycle. This results in an incremental ϕ_{OUT} phase change of 1/2N cycles. The loop phase error ϕ_E may be recovered digitally from the contents of the ÷N counter. For example, a latch circuit strobed by the leading edge of input signal ϕ_{IN} can capture the state of all the ÷N counter bit outputs to obtain a digital reading of $\phi_{IN} - \phi_{OUT}$. The recovered phase resolution is 1/N cycles, as determined by the least significant bit (LSB) of the ÷N counter.

For both analog and digital phase-locked loops using feedback counters, the desired phase resolution does restrict the maximum bandwidth consistent with that resolution and viceversa. The bandwidth of the PLL must be low enough so that the square wave phase detector output, when integrated by the ÷K counter (or by the V_{CO} in the analog case) over 1/2 f_c for ECPD loops or 1/4 f_c for EXORPD loops, will result in less than 1 significant bit phase shift in the feedback counter. Specifically for the DPLL with zero phase error and square wave PD_{OUT}, the K-counter must not recycle more than once for each high or low PD_{OUT} pulse. This will cause every increment pulse at I/D out to be followed by a decrement pulse before the next increment pulse occurs. The alternating increment and decrement pulses will cancel each other, confining the feedback counter phase shift error to 1 significant bit and yielding 1/N phase readout resolution.

If K is too small, the K-counter will supply multiple INCR pulses followed by multiple DECR pulses. The multiple correction pulses will cancel in the higher stages of the ÷N counter, leaving ϕ_{OUT} (MSB) unaffected and zero phase error lock undisturbed. With K too small, however, the ÷N counter lower significant bits fail to average properly the clustered INCR and clustered DECR inputs, giving a false phase error indication from the least significant ÷N bits. This cyclic phase error, called ripple, may be avoided if $K > M/4$ for the EXORPD case and $K > M/2$ for the ECPD case.

For the DPLL circuit without ripple cancellation, this ripple limitation on the phase resolution N imposed by the DPLL bandwidth can be referenced to Q. For the EXORPD circuit of Figure 2(a):

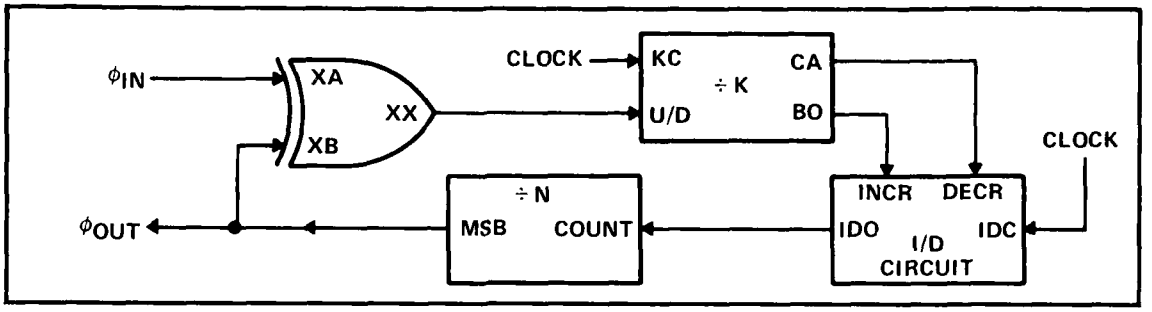
$$N < \frac{8Q}{\pi} \tag{10}$$

For the ECPD case of Figure 2(b):

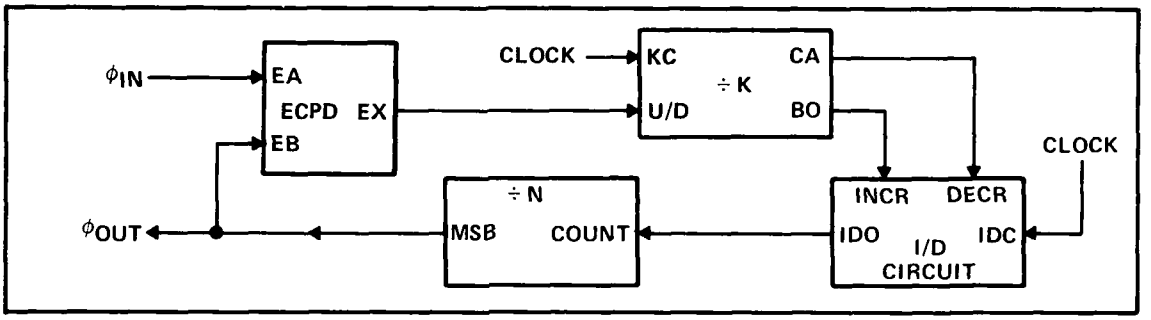
$$N < \frac{2Q}{\pi} \tag{11}$$

Ripple cancellation circuits remove the above restrictions on phase resolution vs bandwidth. Compared to the analog case, ripple cancellation is easily implemented for the DPLL case. Figure 2(c) is a DPLL ripple cancellation circuit using the Exclusive-OR phase detector. The ripple cancellation circuit of Figure 2(d) uses both the EXORPD and the ECPD. With the use of the ENA input in both circuits, the K-counter counts up or down only when phase error correction is needed. The key requirement for eliminating ripple in these circuits is to disable the K-counter when the loop is in lock with zero phase error.

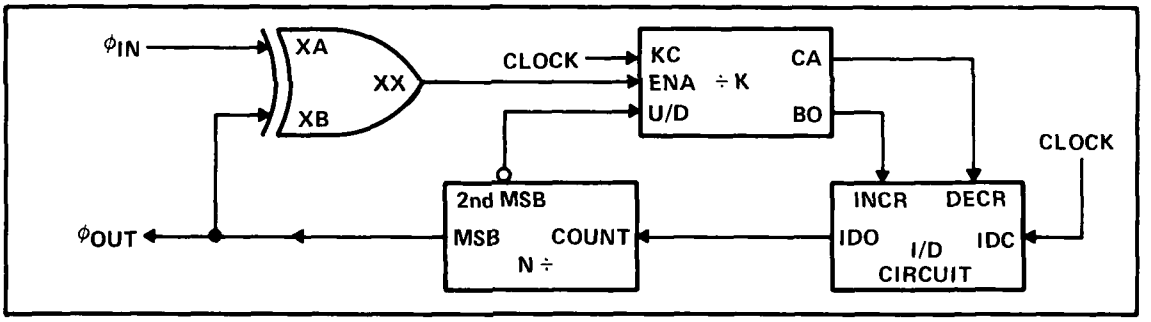
For the circuit of Figure 2(c), the second MSB of the ÷N counter must be a square wave to drive the U/D input to the K-counter; the EXORPD also requires square wave inputs. The phase detector gain K_D is reduced to 2 for this circuit, narrowing the bandwidth accordingly. Also, when $f_{IN} = f_c$, there is 0° phase shift between ϕ_{IN} and ϕ_{OUT} for this circuit. The ripple cancellation circuit of Figure 2(d), with its edge controlled phase detector, can be used where square wave input signals are not available.



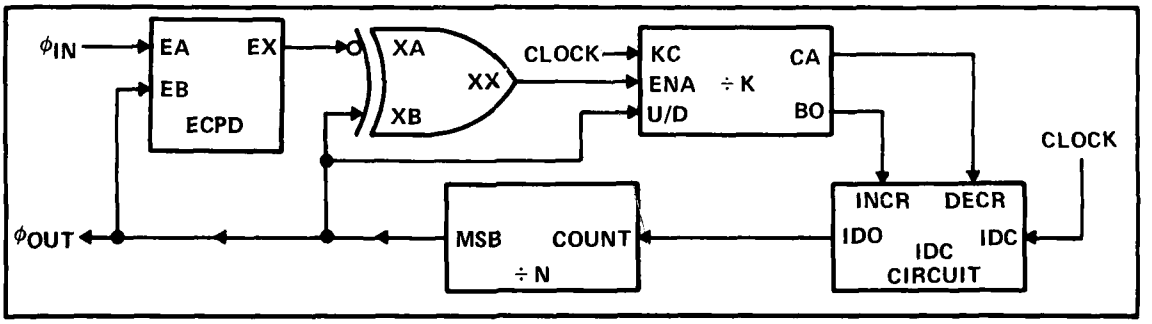
(a) EXCLUSIVE-OR PHASE DETECTOR



(b) EDGE CONTROLLED PHASE DETECTOR



(c) EXORPD WITH RIPPLE CANCELLATION



(d) ECPD WITH RIPPLE CANCELLATION

Figure 2. Digital Phase-Locked Loop Circuit Configurations

F. APPLICATIONS

Strictly speaking, the DPLL is actually a serial digital phase filter (SDPF).[4] The integrated DPLL makes possible digital filtering of phase modulated signals with a minimum of components. The circuits of Figure 2 perform the first-order phase-locked loop function. Higher order filters can easily be implemented by cascading the DPLL circuit. Figure 3 presents a diagram of a second-order phase-locked loop featuring direct readout of phase and frequency data. In a similar manner, n order filters can be formed by cascading n DPLL stages.

The high Q's obtainable with the DPLL IC make the circuit particularly suited for high resolution digital systems. For example, in hyperbolic navigation systems, using multiple phase-locked loops, the DPLL IC can greatly decrease the size and expense of Omega and Loran Receivers.[4] Another suggested application is a resolver-to-digital converter used in aircraft flight controls and numerically controlled machine tools.[5]

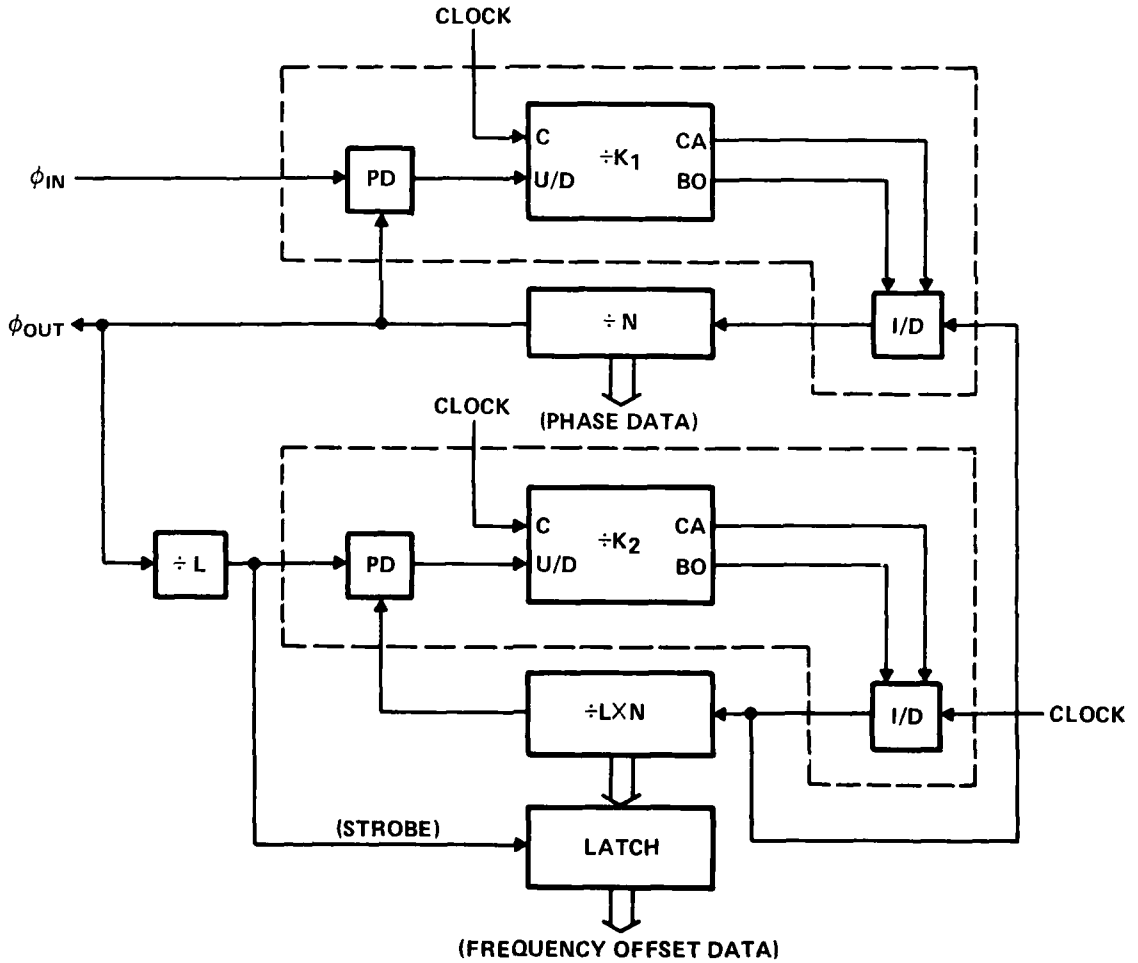


Figure 3. Second Order Digital Phase-Locked Loop with Extended Range and Direct Readout of Phase and Frequency Data[1]

For code tracking and carrier tracking applications, adaptive filters can be constructed using the programmable features of the DPLL IC. The K decoder inputs allow real-time system control of the DPLL bandwidth, and the use of a programmable ÷N feedback counter would extend system control to selection of loop center frequency.

For many phase-locked loop applications, the DPLL has stability and cost advantages over analog alternatives. In communication systems, for instance, the DPLL can provide FM, PSK, and FSK filtering and decoding; clock recovery; and tone recognition. The DPLL is especially adaptable to equipment where the system clock is available as an acceptable frequency reference for loop accuracy. Other suitable areas of application are floppy disk decoders, modems, tape drives, position indicators and servo-controls.

SECTION IV
SN54/74LS297 DIGITAL PHASE-LOCKED LOOP CIRCUIT DESIGN

A. INTRODUCTION

The SN54/74LS297 Digital Phase-Locked Loop (DPLL) integrated circuit implements the functional requirements of the DPLL system as required by the contract and as described by the previous section. The logic of the 16-pin TTL Low Power Schottky IC is shown in Figure 4. The circuit features both Exclusive-OR and Edge Controlled phase detectors, a decode-programmable K-counter with K variable from 2^3 to 2^{17}, an enable input to implement ripple cancellation, and an Increment/ Decrement circuit. For increased flexibility, the DPLL IC does not incorporate a ÷N counter, whose requirements vary with loop center frequency, phase resolution and phase data latch options. The device is designed for −55°C to 125°C full-temperature operation and the inputs and outputs are fully compatible with standard LS TTL specifications.

For maximum marketability, it is important that the DPLL be capable of operating at the highest speed consistent with the device power dissipation limits that reliability imposes. The SN54/74LS297 DPLL was designed with maximum input clock frequency goals of 35 MHz and 50 MHz and a maximum power dissipation goal of 500 mW. To satisfy these requirements, Low Power Schottky TTL technology was specified by the contract to fabricate the DPLL. With standard propagation delays of 8 ns/gate, Low Power Schottky offers a speed-power product below that of any standard production family above 1 MHz (refer to Figure 5). The wide penetration of Low Power Schottky TTL into both military and commercial markets will aid in making the DPLL IC a low-cost-high-volume product.

B. PHASE DETECTOR CIRCUITS

For greater overall system applicability, both the Exclusive-OR phase detector (EXORPD) and the Edge Controlled phase detector (ECPD) are incorporated in this design. The EXORPD offers good noise immunity due to the fact that for phase errors greater than the 90° detection range, the magnitude of the PD output decreases. This effectively narrows the bandwidth of the loop input circuit. The circuit implementation of the EXORPD logic of Figure 4 is shown in the schematic of Figure 6. This configuration was considered best for this application because of minimal signal delay and low power consumption. This is true because an AND-OR gate is constructed as a single gate in TTL, thus giving single-gate speed and power. An active pull-up transistor Q384 is used on the NAND gate output to minimize the race condition existing between the ϕ_A and ϕ_B inputs and the inputs to either AND in the AND-OR gate.

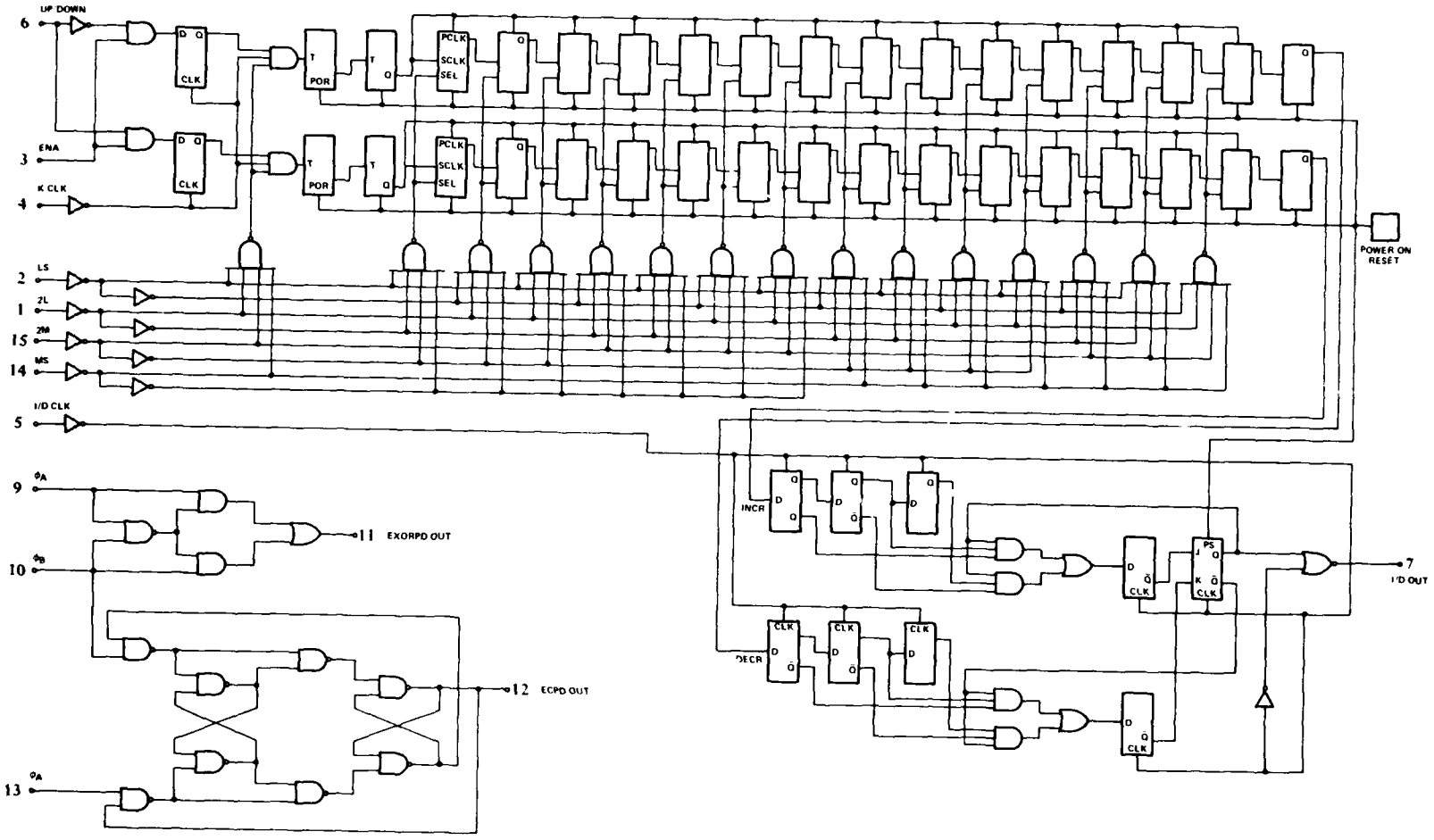


Figure 4. SN54/74LS297 Digital Phase-Locked Loop Logic Diagram

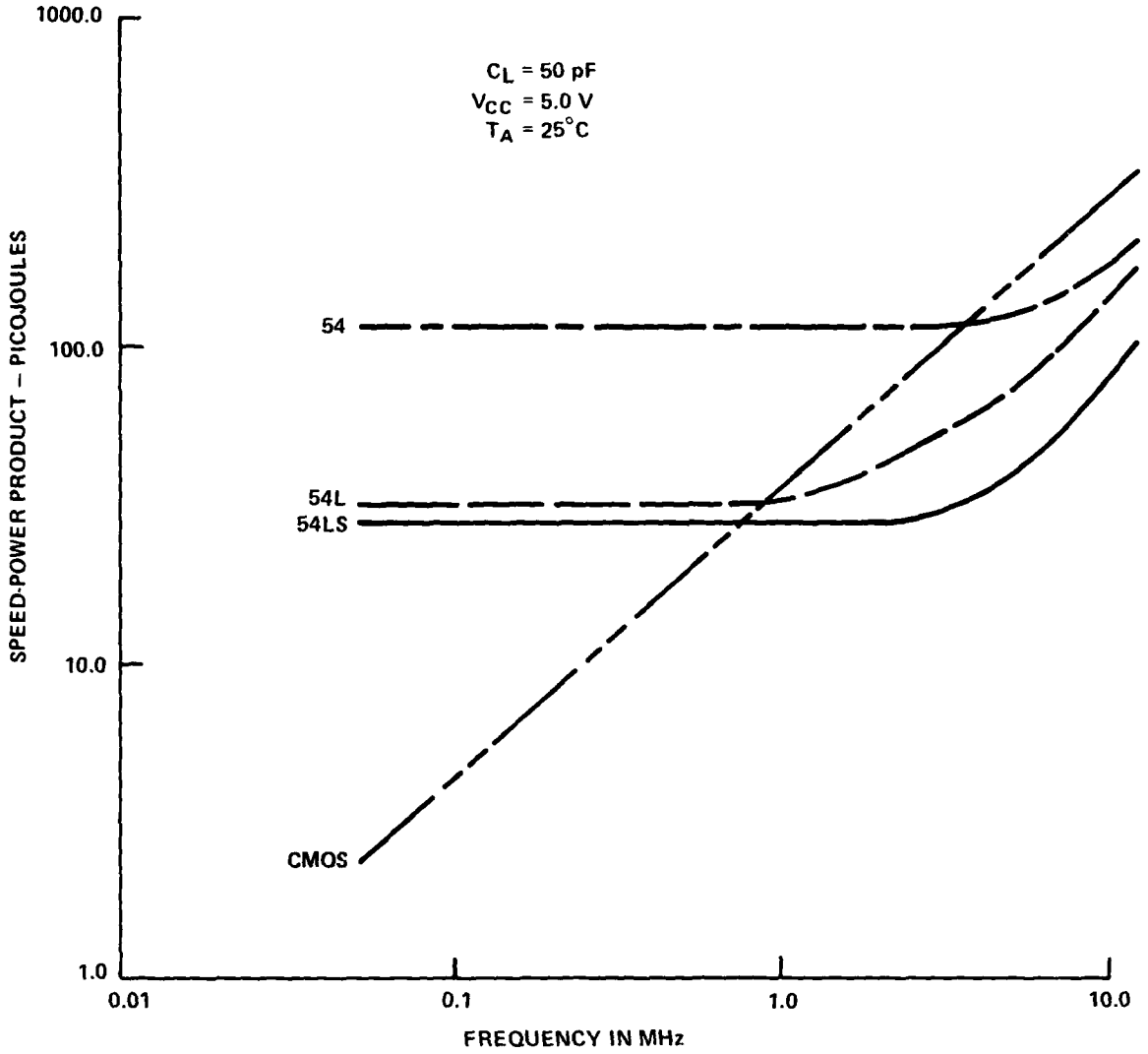


Figure 5. CMOS and TTL Speed-Power Product vs Frequency

The ECPD is included because its wide detection range (±180°) is useful in many applications where noise is not a problem. Also, since the ECPD is edge triggered, there is no requirement that the input be a square wave as in the case of the EXORPD. The ECPD circuit schematic is shown in Figure 7. The circuit is triggered by a negative transition at the ϕ_A' (pin 13) and ϕ_B (pin 10) inputs in such a manner that the ϕ_A' transition causes the output to go low, and the ϕ_B transition causes the output to go high. In normal operation, a one-shot pulse, five delays wide is generated at either of the NAND gate outputs Q395 or Q407. This one-shot signal is long enough to set up the NAND gate crosslatch with inputs Q397 and Q408.

The 16-pin package requirement of the DPLL requires that one input of each phase detector be common. Separate pin-out for the other two inputs allows both phase detectors to be used simultaneously in the ripple cancellation circuit of Figure 2(d).

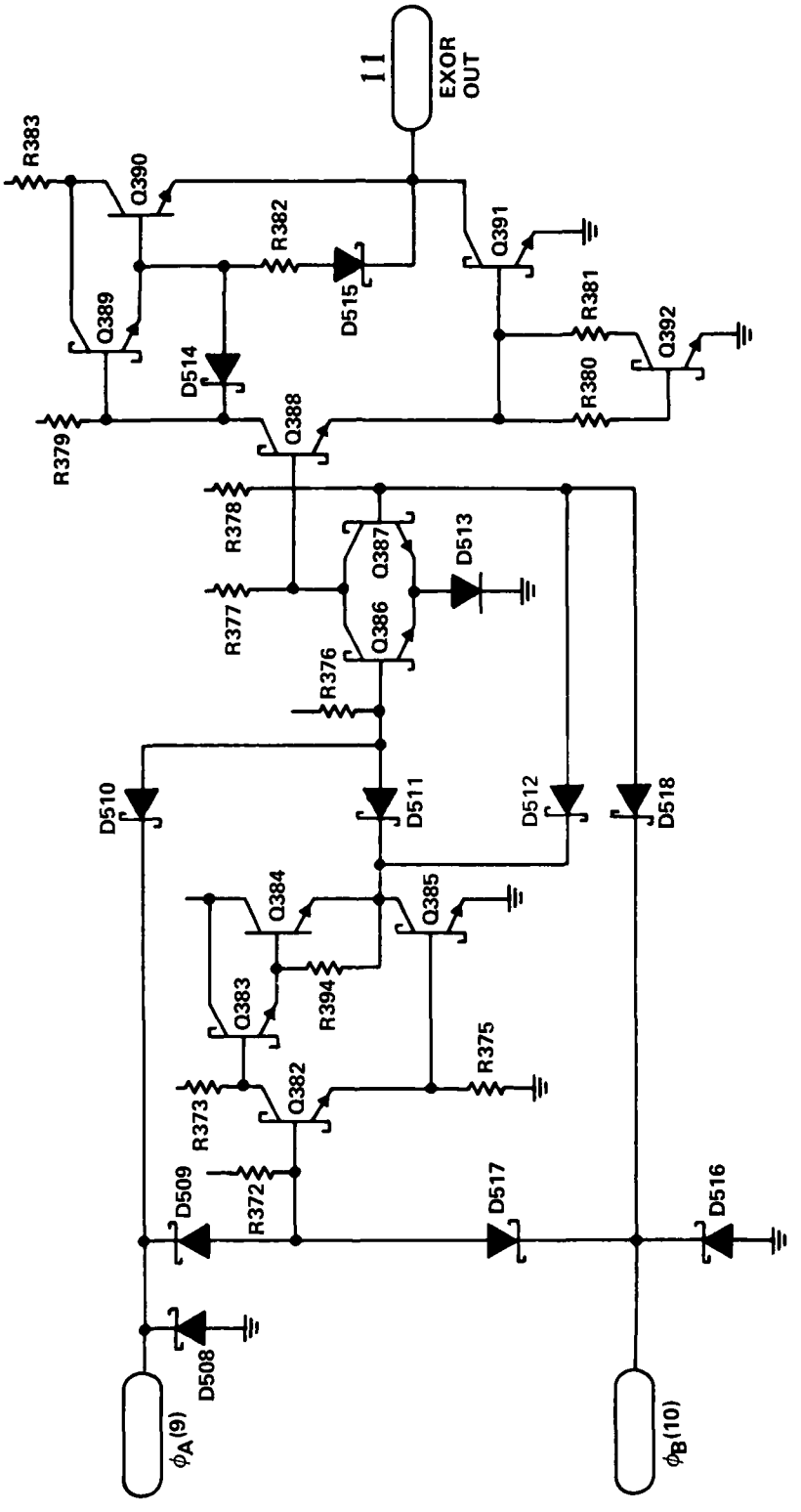


Figure 6. Exclusive-OR Phase Detector Circuit

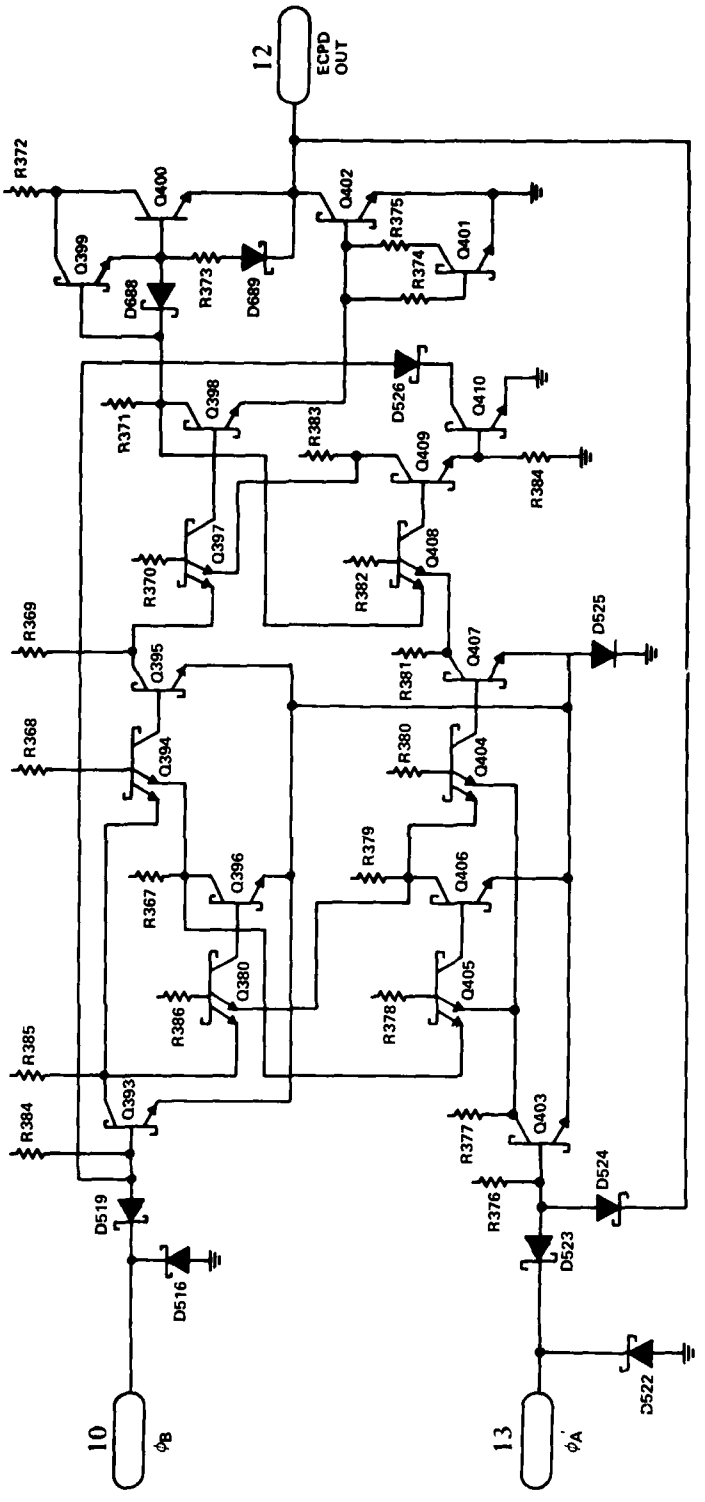


Figure 7. Edge Controlled Phase Detector Circuit

C. K-COUNTER CIRCUIT

Although the K-counter is easily represented as an up/down counter for discussion, this is not the case in implementation. An up/down counter is necessarily a synchronous counter, which limits the maximum clock frequency. The logic required to build an up/down counter of the required size is considerable. The programming method for the K-counter would also add complexity to an up/down counter since bits must be added to or deleted from the least significant bit in order to avoid loss of lock when K is changed. These considerations dictated that the K-counter be implemented as a dual up-counting ripple counter (one for "count up" and one for "count down") with special gating in each flip-flop for programming. Unlike the standard up/down counter, the BO and CA outputs of this counter will continually recycle with a square wave phase detector output. However, the net difference of BO and CA pulses out of the counter will provide the same phase correction of I/D_{OUT} and ϕ_{OUT} as the up/down counter. The amount of ripple is greater with this dual counter scheme, but ripple cancellation can be effectively employed in applications where ripple must be minimized.

Programming the modulus of the K-counter is accomplished by a low true 4-line to 16-line decoder similar in logic to the SN74L154. The 0000 pattern on the K-decoder inputs disables the K-counter. For the other 15 decode positions, the low signal on the selected line disables the ripple carry clock from the preceding counter stage and passes the parallel clock through to the following stage. Table 1 gives the values of K vs the decoder input conditions.

TABLE 1. K-COUNTER MODULUS VS K-DECODER INPUT CONDITIONS

K-Decoder Inputs				K-Counter Modulus
MS (14)	2M (15)	2L (1)	LS (2)	K
0	0	0	0	K-Counter Disable
0	0	0	1	2^3
0	0	1	0	2^4
0	0	1	1	2^5
0	1	0	0	2^6
0	1	0	1	2^7
0	1	1	0	2^8
0	1	1	1	2^9
1	0	0	0	2^{10}
1	0	0	1	2^{11}
1	0	1	0	2^{12}
1	0	1	1	2^{13}
1	1	0	0	2^{14}
1	1	0	1	2^{15}
1	1	1	0	2^{16}
1	1	1	1	2^{17}

The schematic of Figure 8 shows the programmable flip-flop used to implement the variable K feature. Transistors Q1 and Q2 and diodes D9, D10, D11 and D12 comprise the select modulus gating. D12 disables the ripple clock output of the previous stage. Transistors Q3-Q4 and Q5-Q6 form a pair of TTL input gates with a diode (D1-D2) crosslatch for good thermal stability. Feedback toggle data is provided to the two transistor lower latch (Q8-Q9) via diodes D5-D6 and D7-D8. Two diodes are used in each feedback path so that the collectors of Q8 and Q9 will be above the threshold

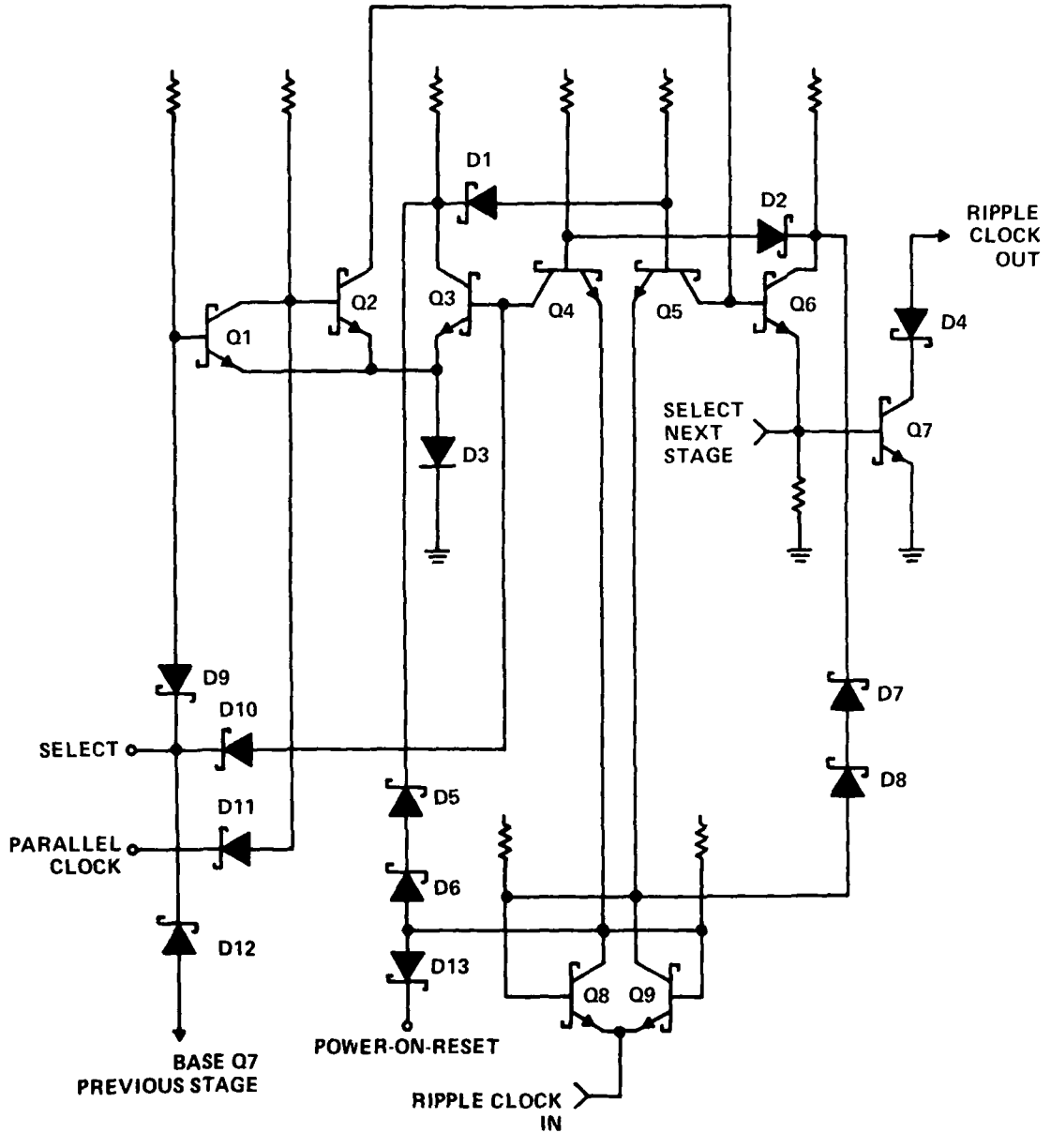


Figure 8. K-Counter Programmable Flip-Flop Circuit

of the upper latch before toggle data can be entered into the lower latch. Data is then transferred to the upper latch on the falling edge of the ripple clock. The power-on-reset (POR) input causes the flip-flop output to set up in the low state when the power is supplied to the IC.

High speed switching at low power is obtained with this type of flip-flop because the logic swings are either minimized or are noncritical. The logic swing at the collector of Q8 for instance is difference between a V_{BE} and a V_{ON}. The collector of Q7 is pulled up through D4 by the logic that it drives, thus eliminating an unnecessarily large voltage swing. The maximum input clock frequency, f_{max}, to any of the programmable flip-flops is limited to one-fourth of the K clock input (pin 4) frequency by the two preceding stages of undecoded high speed flip-flops. This allows the 28 programmable flip-flops to be powered down to less than 3.5 mW each and still obtain an adequate margin of operating speed with an f_{max} greater than 20 MHz.

In order to obtain the desired range of Q, the K-counter has three nonprogrammable flip-flop stages, in addition to the 14 programmable stages. The flip-flop circuit shown in Figure 9 is used for the two counter stages preceding the decodable counter section. This circuit must operate at a higher power dissipation (12 mW) to satisfy the increased operating speed and output drive requirements on the initial K-counter stages.

The circuit of Figure 9 is a negative edge triggered toggle flip-flop with a maximum operating frequency greater than 50 MHz (typical). The operation of the circuit is similar to the toggle section of the programmable flip-flop. Data gate transistors Q18 and Q19 provide the feedback toggle data from the output section to the lower latch transistors Q16 and Q17. The narrow 0.5 V logic swing at the emitters of Q15 and Q20 puts strict requirements on the low level of the internal clock input line, especially for the first counter stage which must run at the full K Clock (pin 4) operating frequency. An active pull-up TTL inverter circuit buffers the pin 4 input to the first counter stage at the proper voltage levels.

The upper latch circuit formed by transistors Q14-15 and Q20-21 limits the maximum input clock frequency. The low time of the internal clock input (emitters of Q16 and Q17) must be greater than the time required by Q14 or Q21 to latch up the output section. This latch-up time is approximately two gate delays or 10 ns at the power level used.

The totem-pole output with Q23 and Q24 is provided for increased speed and also to drive the parallel clock line which has a fan-out of 15.

The K-counter input circuit consists of a pair of D flip-flops with opposite data inputs that synchronize the phase detector output with the K clock, and steer the clock to the appropriate counter. The D flip-flop circuits are similar to the T flip-flop of Figure 9 with the base of Q196 forming the D input when disconnected from the phase splitter Q199 (Figure 10). The disable line from the 0000 K-decoder inputs the AND gates prior to the first K-counter stages to interrupt the K clock signal. The enable input ENA (pin 3) also inputs the AND gates to provide the same K clock disable function when ripple cancellation circuits are connected.

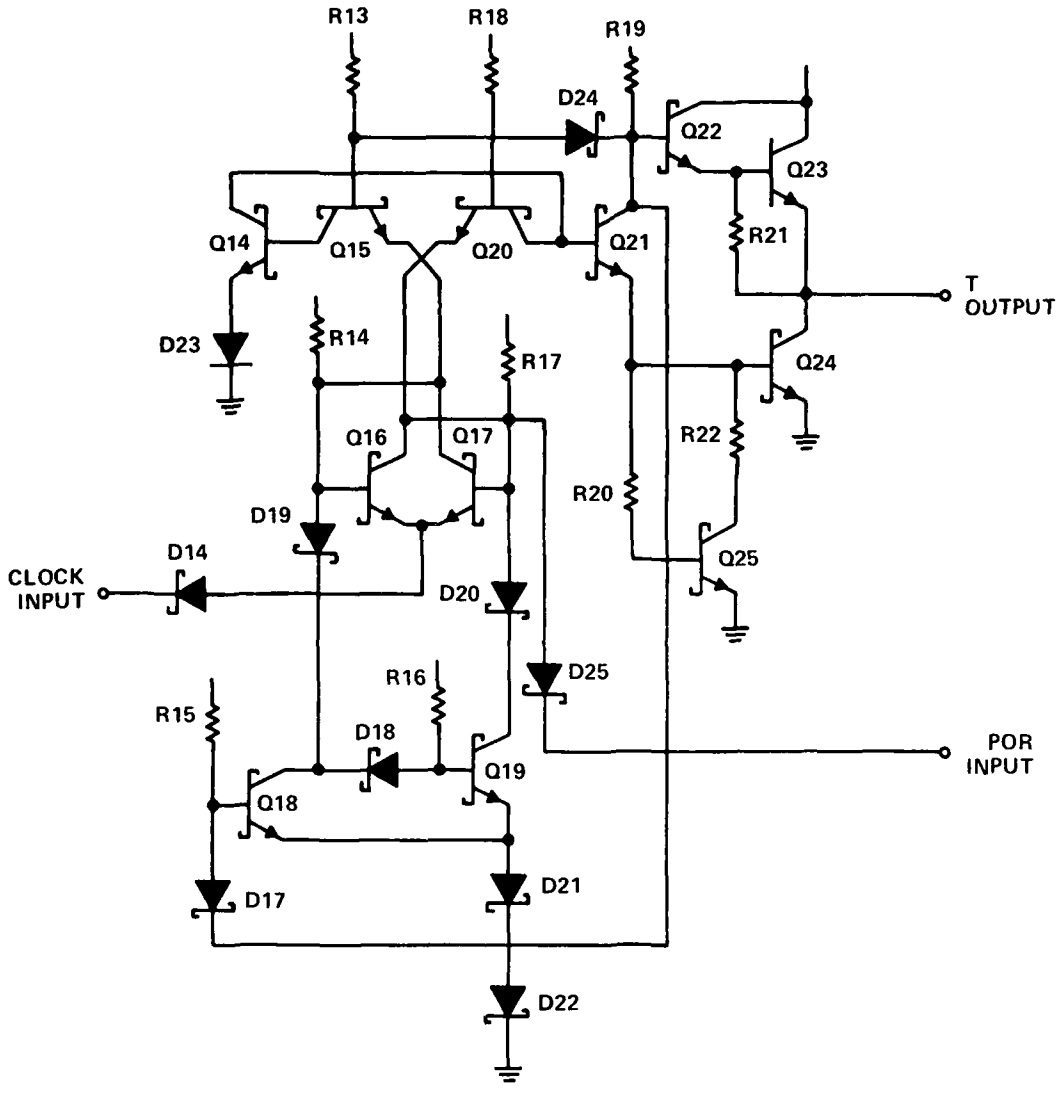


Figure 9. K-Counter T Flip-Flop (Stages 1 and 2)

D. INCREMENT/DECREMENT CIRCUIT

The operation of the Increment/Decrement (I/D) circuit is detailed in Figure 11. A pair of 3-bit shift registers made up of D flip-flops (Figure 10) detect the negative edge of INCR and DECR signals input from the K-counter. The JK flip-flop outputs and the D flip-flop outputs of each shift register are applied to AND-OR gates to generate a one-shot pulse at points C or D for a negative input transition at A or B. Inverting D flip-flops synchronize the one-shot pulse to the J and K inputs of the JK flip-flop, which is similar in design to the flip-flops of Figures 9 and 10. With no signals

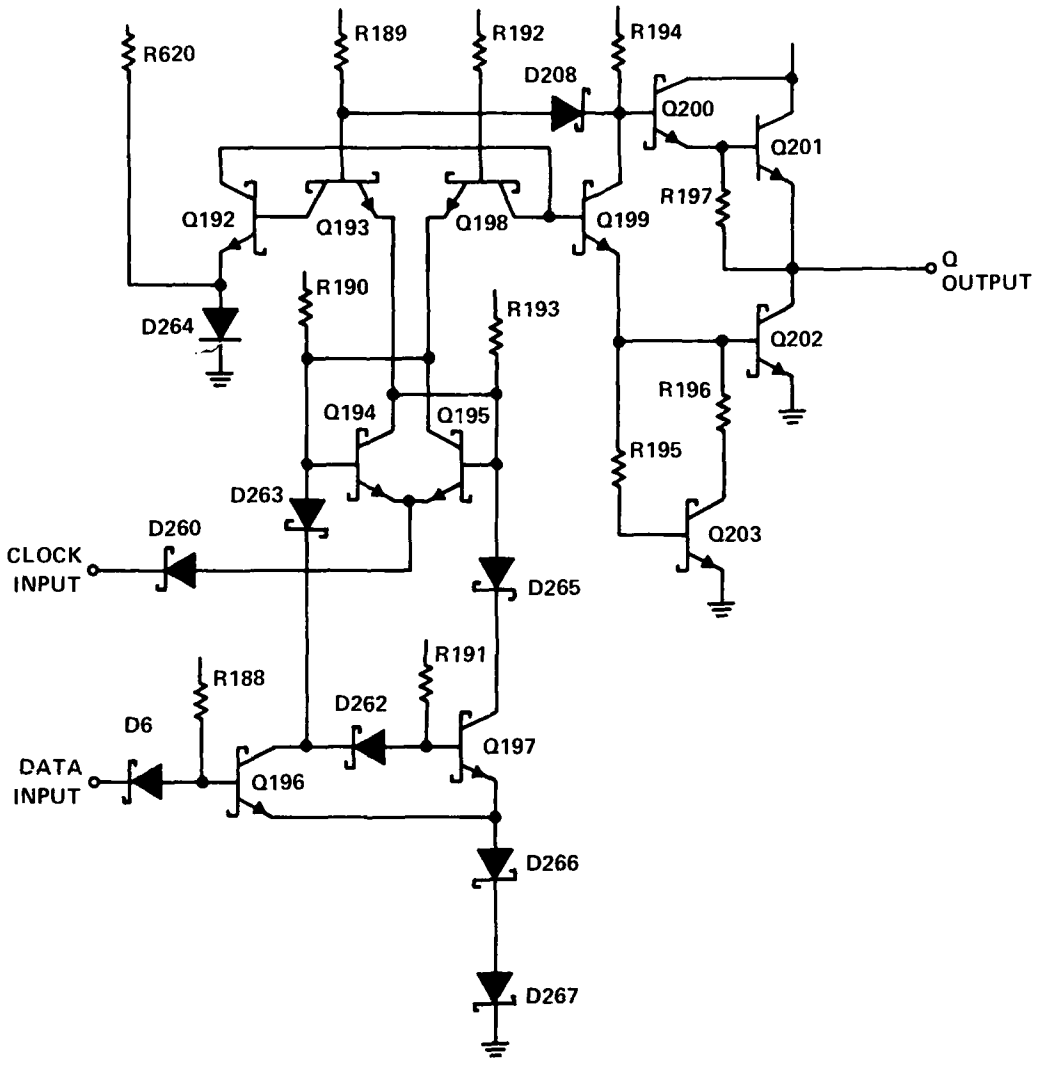


Figure 10. D Flip-Flop Circuit

at the INCR and DECR inputs, the J and K inputs are both high, directing the JK output Q to toggle at 1/2 the I/D CLK (pin 5) frequency. As shown in Figure 11, a negative transition at the INCR input results in a low J input pulse. The JK output Q then remains low for one extra clock period, causing the addition of 1/2 cycle to the I/D OUT waveform. Similarly, a negative DECR pulse results in a low K input pulse and a net decrement of 1/2 cycle for I/D OUT.

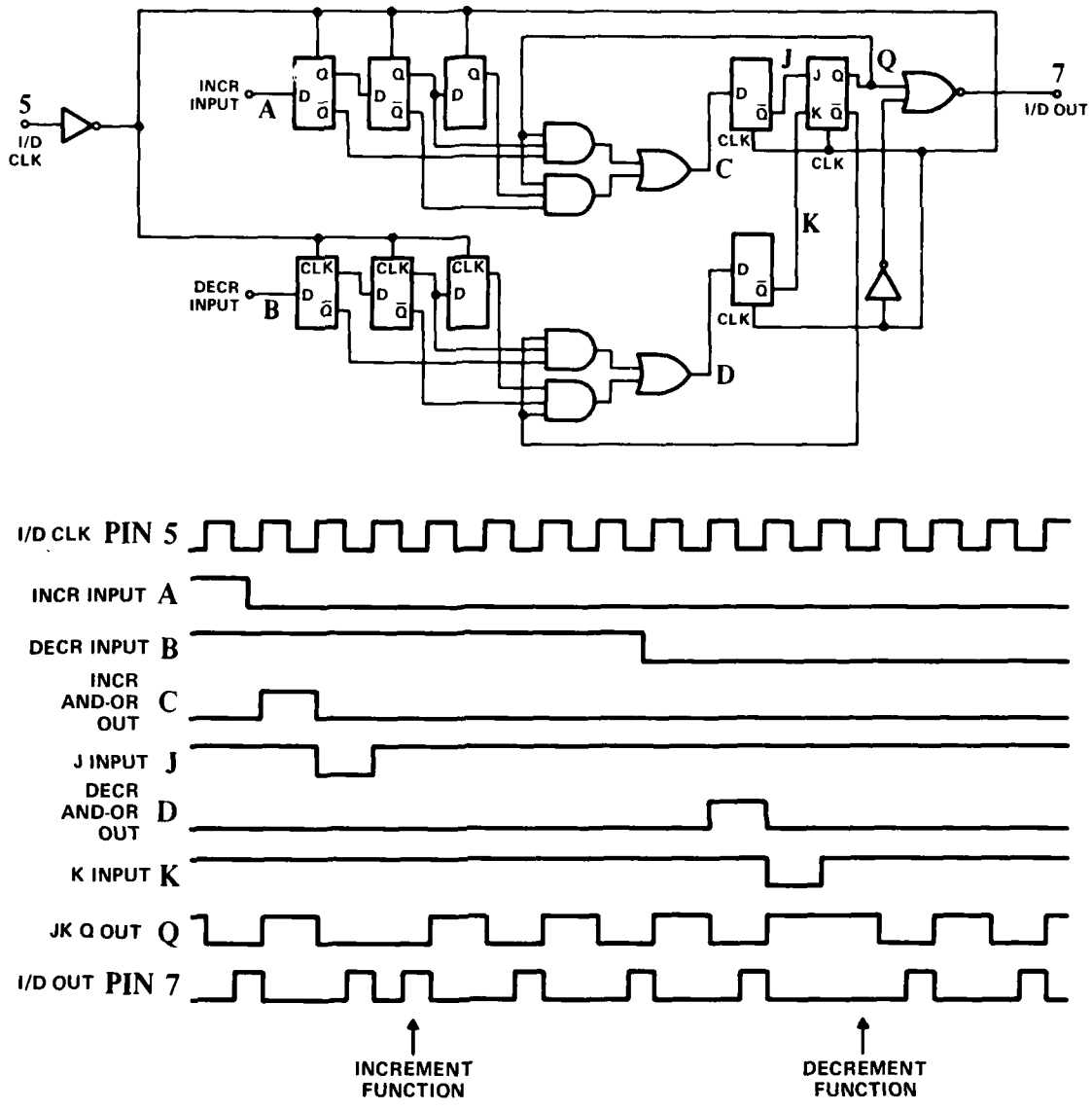


Figure 11. Increment/Decrement Circuit Waveforms

The maximum operating frequency of the I/D circuit is limited by the speed of the shift register section. The minimum period of the I/D clock input signal must be longer than the time required to shift data from one D flip-flop to the next. This time is equal to the output propagation delay plus the D input set-up time. This time requirement limits the f_{max} (typical) of the I/D clock to 35 MHz.

The I/D output circuit is shown in Figure 12. This circuit is similar to the phase detector outputs but with the power increased to meet the greater load requirements. The I/D OUT maximum rated load currents are 12 mA sink and 1.2 mA source compared to the phase detector output specifications of 4 mA sink and 400 μA source.

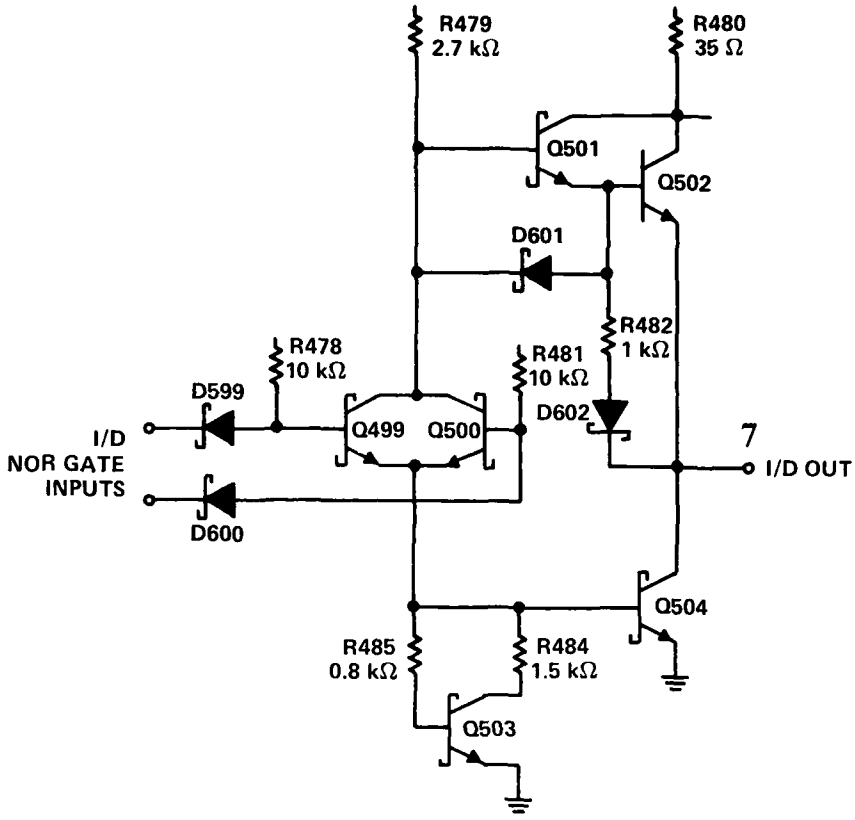


Figure 12. Increment/Decrement Circuit Output Buffer

SECTION V
DEVICE FABRICATION

A. BAR DESCRIPTION

Fabrication of the SN54/74LS297 (hereinafter referred to as 'LS297) Digital Phase-Locked Loop (DPLL) was accomplished in accordance with the requirements of contract section 4.2. Figure 13 is a photograph of the completed DPLL IC. The 'LS297 device has approximately 1900 components and bar dimensions of 194 X 95 mils. The large repetitive area at the center of the bar contains the dual 17-stage programmable K-counter. The cellular section to the right of center is comprised of Increment/Decrement circuit flip-flops. In addition to its 16 bond pads, the 16-pin device has four internal test pads (A-D) to reduce test time at wafer probe. Pin functions for the 'LS297 DPLL are given in Figure 14.

B. DESIGN PROCEDURE

The DPLL was integrated according to standard 54/74 Low Power Schottky design procedures. The device logic (Figure 4) and pin-out (Figure 14) were approved by the contractor to meet the DPLL function requirements.

Circuit simulation for the SN54/74LS297 was done on a logic and a component level. An effort was made to improve the DPLL operation by designing and simulating a synchronous up/down counter for the programmable K-counter section. Factors of components count and operating speed caused the up/down counter design to be abandoned in favor of the dual ripple counter originally proposed and approved. In addition to logic simulation and verification of the DPLL IC, a TTL breadboard of the I/D circuit was constructed to check operation of the design. Using the circuits discussed in Section IV, the 'LS297 logic was implemented according to established circuit design practices.

The dc and ac performance of the 'LS297 circuits was simulated at the component level by SPICE computer analysis. This software program applies empirically determined transistor and diode component models to circuit description input data in order to compute the dc operating point of all circuit nodes. SPICE computes the transient response to input pulses and provides plots of output waveforms to predict design switching speeds. The DPLL circuit simulation determined the proper component values for military range device operation, with simulations done for power supply variations of 4.5 V to 5.5 V and temperature variations of −55°C to 125°C.

Considerable SPICE analysis was done to optimize the maximum operating frequency of the high-speed flip-flop circuits (Figures 9 and 10). Component sizes were adjusted for maximum toggle frequency consistent with power limitations and reliable voltage swings. Simulations of these flip-flop circuits indicated a maximum input clock frequency of 50 MHz, the design goal of this project.

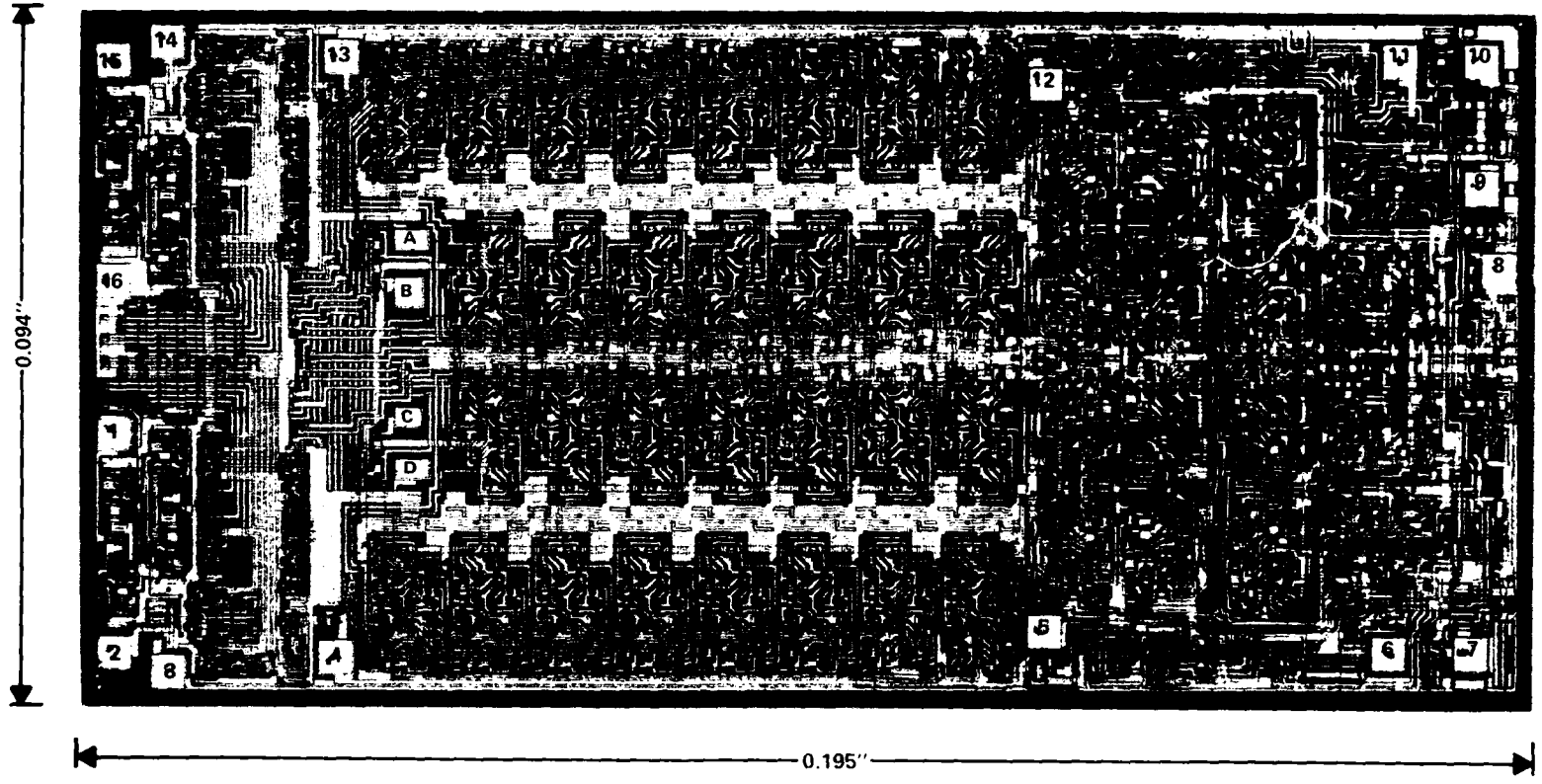


Figure 13. SN54/74LS297 Digital Phase-Locked Loop Bar

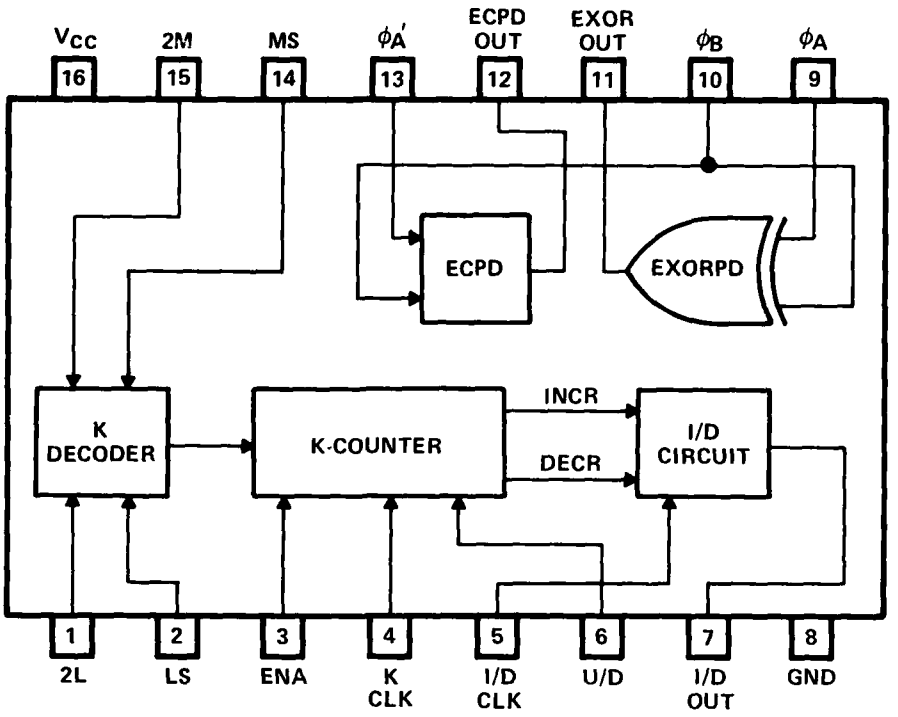


Figure 14. SN54/74LS297 Digital Phase-Locked Loop Pin Assignments

C. BAR LAYOUT AND MASK GENERATION

Layout of the SN54/74LS297 circuits achieved a packing density of 10 square mils per component. A key factor in this high TTL packing density was the use of two-level metal interconnects and cellular structures. Each type of flip-flop was designed as a cell with minimum area and repetitively positioned on the DPLL bar layout. Second-level metal bus lines running over the flip-flop cells provide interconnection of the cells without additional bar area. If the DPLL circuit had used only single-level metallization, these control lines could not have been run over active components, and additional bar area would have been required for bus line routing. Manufacturing data indicates that for large circuits, the reduced bar area of two-level metal layout results in higher probe test yield compared to single-level metal design. The extensive use of cells on the 'LS297 bar also descreased bar layout time and simplified bar layout checkout.

The data files for the DPLL masks were created by digitizing the 'LS297 layout drawings and editing results on a CRT graphics terminal. Computer generated plots of each IC level were checked out with the aid of a design rule verification computer program to indicate device geometry errors. After completing correction of all layout errors, tapes were released to generate masks for the DPLL IC. Optically generated 100X color transparencies of each IC level were obtained during the mask fabrication to provide a final design check of DPLL component dimensions and connections.

D. MATERIAL PROCESSING

The prototype lot of SN54/74LS297 material was processed in the Low Power Schottky production facility according to standard LS manufacturing specifications. The mask list for this prototype material is given in Table 2. Completed DPLL material was tested and assembled in 16-pin packages for shipment to the AFAL as required by this contract.

TABLE 2. SN54LS297 MASK LIST

Mask Number	Mask Level	Mask Type
856-640B	DUF	Chrome
856-641B	Isolation	Chrome
856-642B	Isolation-2nd Coat	Chrome
856-643C	Base	Chrome
856-645B	Resistor	Chrome
856-646B	Emitter	Chrome
856-647B	Contacts	Chrome
861-390B	Contacts-2nd Coat	Chrome
856-655D	Leads 1 Mask Array	Iron Oxide
856-659C	Leads 2 Mask Array	Iron Oxide
856-660A	Nitride Passivation	Iron Oxide

SECTION VI
SN54/74LS297 DIGITAL PHASE-LOCKED LOOP PERFORMANCE TESTS

A. INTRODUCTION

The SN54/74LS297 Digital Phase-Locked Loop Integrated Circuit was tested according to standard SN54/74LS test procedures and as required by paragraph 4.3 of the contract. The device successfully met all dc and ac performance requirements. Fifty-five SN54LS297J ceramic packaged devices and 55 SN74LS297N plastic packaged devices were shipped to the AFAL for evaluation. Each ceramic packaged device was tested for adherence to dc and ac performance requirements of the Statement of Work at - 55°C, 25°C and 125°C. Each plastic packaged device was fully tested at 25°C. Documentation of test results for each unit delivered was supplied to the AFAL.

B. DPLL FUNCTIONAL TEST PROGRAM

A functional test program for the SN54/74LS297 DPLL has been implemented on the Texas Instruments Advanced Technology Test System (ATT-2). This integrated circuit test program tests complete functionality of the DPLL device as defined by the LS297 logic diagram (Figure 4).

The first step of the test program is to test the phase detector circuits according to the Truth Tables given (Tables 3 and 4). The Exclusive-OR phase detector (EXORPD) is tested by applying the four input pin patterns listed and by checking the output pins for the correct logic level. The Edge Controlled phase detector (ECPD) is negative edge triggered. The ECPD output (pin 12) is set to a "1" by a negative edge applied to pin 10. Likewise, a negative transition applied to pin 13 causes the ECPD output to be reset to a "0" logic level. The sequence of input patterns and required output test patterns is given in Table 3 (EXORPD) and in Table 4 (ECPD).

The K-counter and Increment/Decrement circuits are tested simultaneously for all K-counter decode positions as outlined in Table 5. The K-decoder inputs determine the proper count of pulses applied to the clock inputs (pins 4 and 5) prior to test of the I/D output (pin 7) for an incremented or decremented waveform (Figures 15 and 16). The logical state of the Up/Down input determines whether an increment (pin 6 low) or a decrement (pin 6 high) function is performed. The disable function is tested by verifying that the K-counter contents are not altered when the enable pin (3) is low.

The ATT-2 test program was successfully used to test the DPLL IC both at wafer probe and post assembly. DPLL test yield was consistent with standard Low Power Schottky test yields for two-level metal devices with the same bar area. One problem with the test program was excessive test time due to the test of the 17-stage K-counter. For production purposes, the test program will be revised to make use of four internal test pads provided on the DPLL bar at wafer probe. These pads allow the long K-counter to be tested in two sections, reducing K-counter test time by several orders of magnitude.

TABLE 3. TRUTH TABLE
SN54/74LS297 EXCLUSIVE-OR PHASE DETECTOR

ϕ_A Input Pin 9	ϕ_B Input Pin 10	EXORPD Output Pin 11
0	0	0
1	0	1
0	1	1
1	1	0

TABLE 4. TRUTH TABLE
SN54/74LS297 EDGE CONTROLLED PHASE DETECTOR

ϕ_B Input Pin 10	ϕ_A' Input Pin 13	ECPD Output Pin 12
1	0	X
0	1	X
0	1	1
1	0	0
0	1	1
1	0	0

NOTES: Low Level Input, $V_{I0} \leq .7$ V, High Level Input $V_{I1} \geq 2$ V
Low Level Output, $V_{O0} \leq .4$ V; High Level Output $V_{O1} \geq 2.7$ V
X = No Test (Set-Up Pattern)

C. DC PARAMETRIC TEST OF INPUT/OUTPUT SPECIFICATIONS

Tables 6 and 7 list the recommended operating conditions and the tested electrical characteristics for the SN54/74LS297 evaluation devices produced under the DPLL contract. These specifications comply with the test limits and test conditions required by contract section 4.4. These dc performance characteristics were measured after functional test by the same ATT-2 test program at −55°C, 25°C and 125°C. A computer printout was produced listing the test data on each unit shipped as well as lot summaries and distribution plots for each test parameter. SN54/74LS297 test results indicated excellent dc parametric yield over the required temperature and voltage operating range.

D. SAMPLE AC CHARACTERIZATION OF MAXIMUM INPUT CLOCK FREQUENCY

The maximum operating frequency of the K clock and I/D clock inputs was measured for a sample of units passing the dc functional and parametric tests. The I/D clock input was tested according to the test diagram of Figure 17. A frequency counter was used to monitor the ratio of the I/D output frequency to the I/D clock input frequency. The DPLL operated in a constant increment or constant decrement mode, depending on the voltage applied to the Up/Down input (pin 6). All K-counter decode inputs were switched high to fully exercise the entire K-counter

TABLE 5. K-COUNTER AND I/D CIRCUIT FUNCTIONAL TEST PROCEDURE

ATT-2 Test Name	Decode Pins 2 1 15 14	ENA Pin 3	U/D Pin 6	No. of K CLK (4) Pulses Before Test of I/D Out	Function of I/D Out (7) During Test	Test Description
FUN01	1000	1	1	0	$I/D_{CLK} \div 2$	Clear I/D Circuit (6 I/D CLK Pulses)
NUF01	1000	1	1	7	Decrement	Decrement: $K=2^3$
	1000	1	1	8	Function	(See Figure 16 for Waveform)
DIS1	1000	0	1	30	$I/D_{CLK} \div 2$	Disable DECR Function
DIS2	1000	1	0	7	Increment	Increment: $K=2^3$
	1000	1	0	8	Function	(See Figure 15 for Waveform)
	1000	0	0	30	$I/D_{CLK} \div 2$	Disable INCR Function
FUN02	0100	1	1	15	Decrement	Decrement $K=2^4$
	0100	1	0	15	Increment	Increment
FUN03	1100	1	1	31	Decrement	Decrement $K=2^5$
	1100	1	0	31	Increment	Increment
FUN04	0010	1	1	63	Decrement	Decrement $K=2^6$
	0010	1	0	63	Increment	Increment
FUN05	1010	1	1	127	Decrement	Decrement $K=2^7$
	1010	1	0	127	Increment	Increment
FUN06	0110	1	1	255	Decrement	Decrement $K=2^8$
	0110	1	0	255	Increment	Increment
FUN07	1110	1	1	511	Decrement	Decrement $K=2^9$
	1110	1	0	511	Increment	Increment
FUN08	0001	1	1	1023	Decrement	Decrement $K=2^{10}$
	0001	1	0	1023	Increment	Increment
FUN09	1001	1	1	2047	Decrement	Decrement $K=2^{11}$
	1001	1	0	2047	Increment	Increment
FUN10	0101	1	1	4095	Decrement	Decrement $K=2^{12}$
	0101	1	0	4095	Increment	Increment
FUN11	1101	1	1	8191	Decrement	Decrement $K=2^{13}$
	1101	1	0	8191	Increment	Increment
FUN12	0011	1	1	16383	Decrement	Decrement $K=2^{14}$
	0011	1	0	16383	Increment	Increment
FUN13	1011	1	1	32767	Decrement	Decrement $K=2^{15}$
	1011	1	0	32767	Increment	Increment
FUN14	0111	1	1	65537	Decrement	Decrement $K=2^{16}$
	0111	1	0	65537	Increment	Increment
FUN15	1111	1	1	131064	$K_{CLK} \div 2$	Begin DECR Test; $K=2^{17}$
	0000	1	1	60	$K_{CLK} \div 2$	Decode 0000 Disable (No DECR Occurs)
	1111	1	1	5	Decrement	Decrement Occurs; $K=2^{17}$
	1111	1	0	131064	$K_{CLK} \div 2$	Begin INCR Test $K=2^{17}$
	0000	1	0	60	$K_{CLK} \div 2$	Decode 0000 Disable (No INCR Occurs)
	1111	1	0	5	Increment	Increment Occurs $K=2^{17}$ End Functional Test, Branch to DC Parametric Test

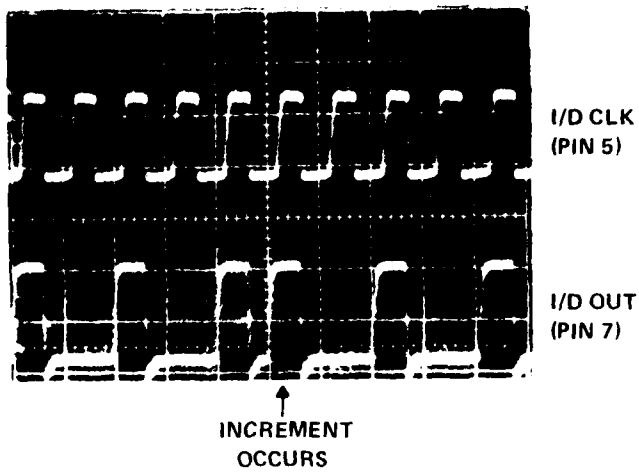


Figure 15. I/D Output Waveform – Increment Function

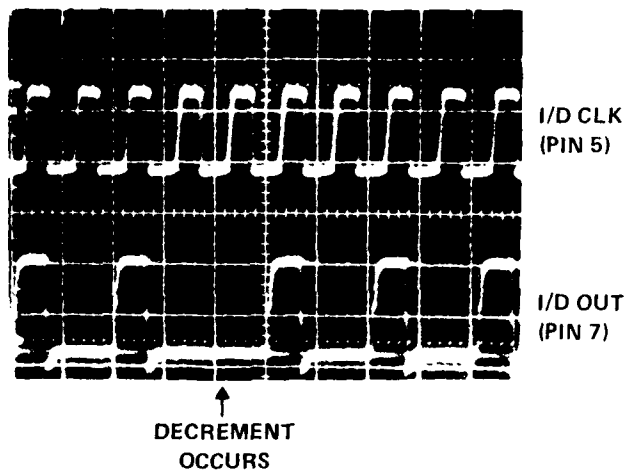


Figure 16. I/D Output Waveform – Decrement Function

TABLE 6. SN54/74LS297 DPLL RECOMMENDED OPERATING CONDITIONS

		SN54LS297			SN74LS297			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	I/D Output			−1.2			−1.2	mA
	PD Outputs			−400			−400	μA
Low-level output current, I_{OL}	I/D Output			12			24	mA
	PD Outputs			4			8	mA
Operating free-air temperature, T_A		−55		125	0		70	°C
Storage Temperature, T_s		−65		150	−20		95	°C

TABLE 7. SN54/74LS297 DPLL ELECTRICAL CHARACTERISTICS OVER RECOMMENDED FREE-AIR TEMPERATURE RANGE

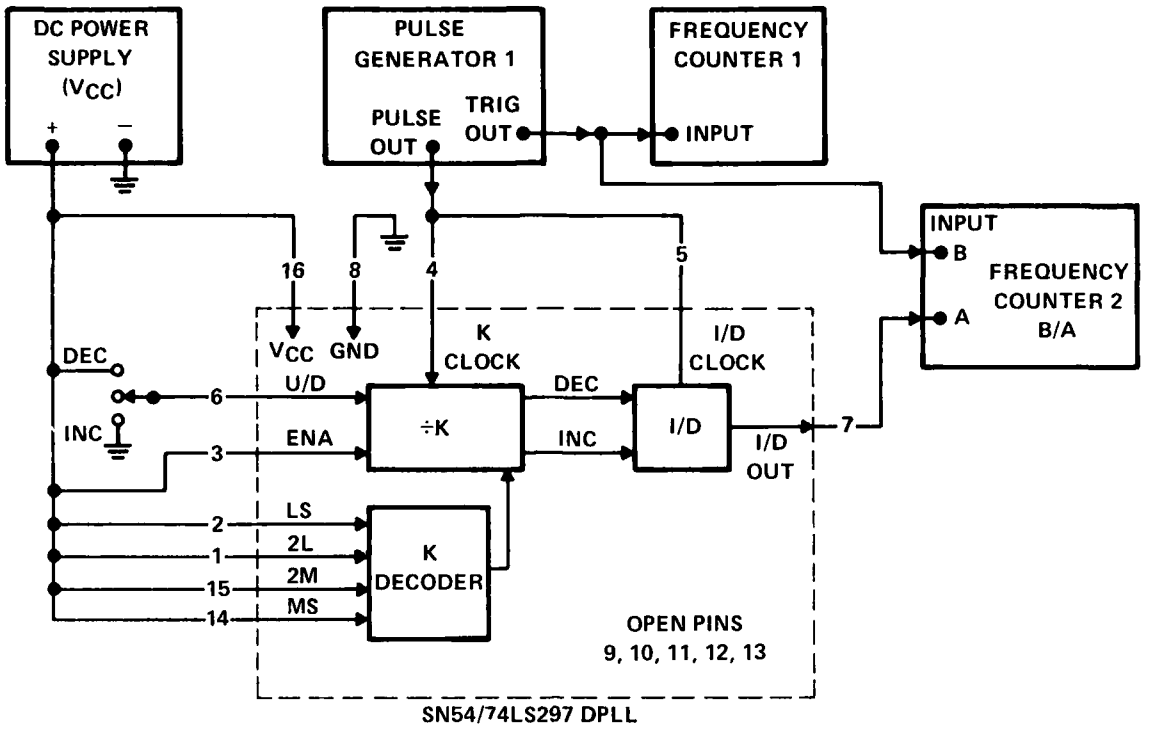
PARAMETER		TEST CONDITIONS*			SN54LS297			SN74LS297			UNIT
					MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = −18 mA				−0.9	−1.5		−0.9	−1.5	V
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IH} = 2 V, V_{IL} = $V_{IL\ max}$	I/D Out	I_{OH} = Max	2.5	2.95		2.5	3.15		V
			PD Out	I_{OH} = Max	2.5	2.95		2.5	3.15		
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IH} = 2 V	I/D Out	I_{OL} = 12 mA		0.32	0.4		0.29	0.4	V
				I_{OL} = 24 mA					0.39	0.5	
			PD Out	I_{OL} = 4 mA		0.30	0.4		0.28	0.4	
				I_{OL} = 8 mA					0.36	0.5	
I_I	Input current at maximum input voltage	V_{CC} = Max, V_I = 7 V				1	100		1	100	μA
I_{IH}	High-level input current	V_{CC} = Max, V_I = 2.7 V				1	20		1	20	μA
I_{IL}	Low-level input current	V_{CC} = Max, V_I = 0.4 V	ϕ_A, CLOCKS, ENA, U/D			−0.48	−0.8		0.49	−0.8	mA
			ϕ_B			−0.45	−1.2		−0.47	1.2	
			All other inputs			−0.23	−0.4		−0.23	0.4	
I_{OS}	Short-circuit output current††	V_{CC} = Max	I/D Output		−30	76	−130		76	−130	mA
			PD Outputs		−20	50	−100		50	−100	
I_{CC}	Supply current	All inputs grounded, All outputs open	V_{CC} = Max			81	120		85	120	mA
			V_{CC} = 5 V			72	100		75	100	

*For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions.

†All typical values are at specified V_{CC}, T_A = 25°C (test data from evaluation lots no. 419 (SN54LS297J) and no. 393 (SN74LS297N).

††Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

AC TEST DIAGRAM 1



TEST EQUIPMENT	
PULSE GENERATOR 1	HEWLETT PACKARD 8082A OR EQUIV ($f_{out} \geq 50$ MHz; t_r, $t_f \leq 2$ ns)
FREQUENCY COUNTER 1	TEKTRONIX DC503 OR EQUIV
FREQUENCY COUNTER 2	HEWLETT PACKARD 5345A OR EQUIV (B/A FUNCTION $f_{in} \geq 35$ MHz FOR INPUTS A & B)
DC POWER SUPPLY	TEKTRONIX PS503A OR EQUIV (4.5-5.5 V, 200 mA)
TEMPERATURE TEST CHAMBER	STATHAM SD6-1
TEMPERATURE MONITOR	DORIC TRENDICATOR 400A TYPE J/°C

Figure 17. SN54/74LS297 AC Performance Test Diagram
Maximum Input Frequency Test – I/D Clock Input (Pin 5)

chain during the test. The $I/D_{IN} \div I/D_{OUT}$ frequency ratio R is independent of the input clock frequency and a function only of the K-counter decode K, the ratio of K clock to I/D clock input frequencies M/2N, and the function selected (increment or decrement). The ratio R can be calculated according to:

$R = 2 + 2(M/2N)/K$ Decrement Mode (U/D High)
$R = 2 \quad 2(M/2N)/K$ Increment Mode (U/D Low)

For:

$$K = 2^{17} \text{ (All Decode Inputs High)}$$
$$M/2N = \text{One (Clock Inputs Common)}$$
$$R = 2.000015259 \text{ (Decrement Mode)}$$
$$R = 1.999984741 \text{ (Increment Mode)}$$

Each unit was characterized by recording the maximum I/D clock input frequency that yielded the correct input/output ratio R as specified above.

In like manner, the K clock maximum input frequency was characterized according to the test diagram of Figure 18. The I/D clock input frequency was equal to 1/2 the K clock input frequency to avoid limiting of f_{max} by the I/D clock input. The $I/D_{IN} \div I/D_{OUT}$ frequency ratio R was again used to verify the maximum input frequency to the K clock. For this case M/2N = 2 and R becomes:

$$R = 2.000030518 \text{ (Decrement Mode)}$$
$$R = 1.999969482 \text{ (Increment Mode)}$$

A summary of f_{max} characterization data for the full operating ranges of voltage and temperature is listed in Table 8. For the evaluation lot of SN54LS297 devices, the average K clock maximum input frequency varied between a typical value of 56 MHz (5 V, 25°C) and a worst case value of 39 MHz at 5.5 V, 125°C. The I/D clock maximum input frequency varied between a typical 35 MHz and a worst case f_{max} of 21 MHz (5.5 V, 125°C). For the 0° to 70°, 4.75 V to 5.25 V operating range of the SN74LS297, the data projected an average K clock f_{max} of 50 MHz and a 30 MHz I/D clock f_{max}.

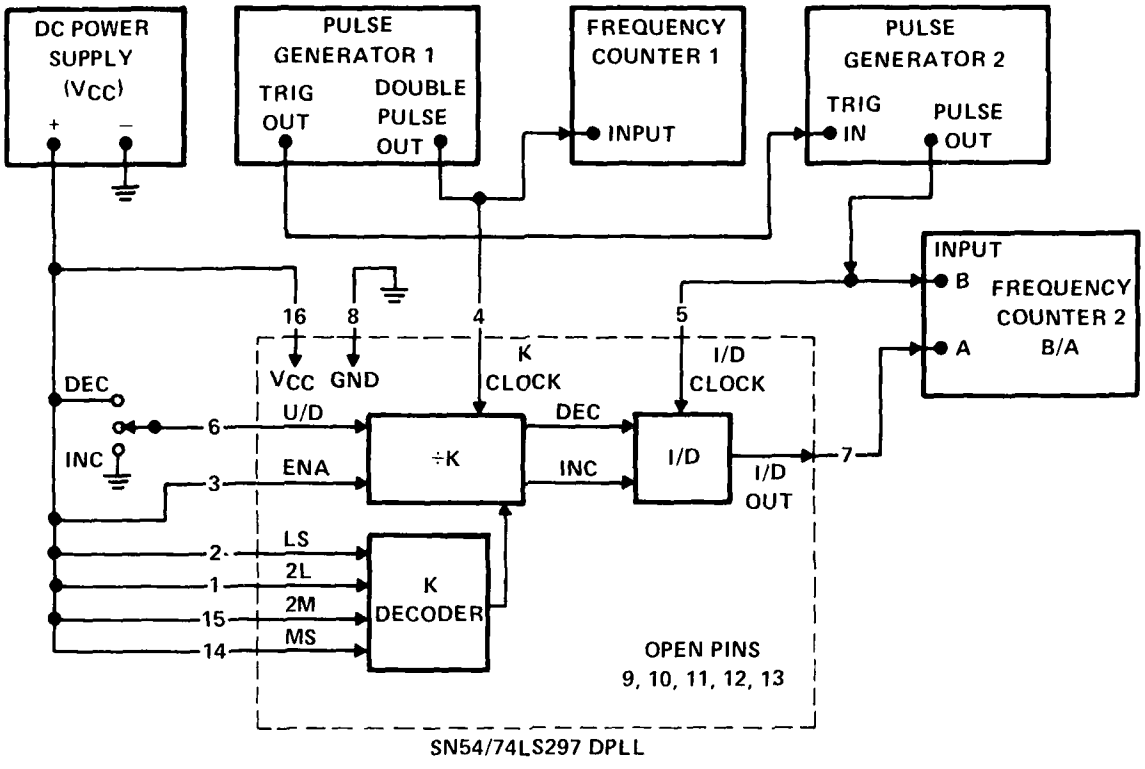
E. AC FINAL TEST

All SN54LS297J ceramic packaged DPLL devices shipped under this contract were tested for worst case maximum clock input frequency f_{max} over the 4.5 V to 5.5 V supply range and over the -55°C to 125°C temperature range. This f_{max} test was carried out using the test procedure and test equipment described for the f_{max} characterization data of the previous section. According to the DPLL design review with the AFAL on 1 August 1979, the test limits of worst case f_{max} were 30 MHz for the K clock input and 15 MHz for the I/D clock input. Of 76 good dc tested SN54LS297 units, 65 units passed this ac performance test.

All plastic and ceramic units shipped were tested for a typical f_{max} of 50 MHz for the K clock input and a f_{max} of 35 MHz for the I/D clock input. This test was made at typical operating conditions (5 V, 25°C). Of the evaluation lot devices which tested good functionally and dc parametrically, 98% passed this f_{max} (typical) test.

A listing of the SN54/74LS297 switching characteristics is presented in Table 9. A final determination of product data sheet specifications will be made after evaluation of additional characterization material is completed.

AC TEST DIAGRAM 2



TEST EQUIPMENT

PULSE GENERATOR 1	HEWLETT PACKARD 8082A OR EQUIV ($f_{out} \geq$ 50 MHz, t_r, $t_f \leq$ 2 ns)
PULSE GENERATOR 2	TEKTRONIX PG508 OR EQUIV ($f_{out} \geq$ 50 MHz, t_r, $t_f \leq$ 5 ns)
FREQUENCY COUNTER 1	TEKTRONIX DC503 OR EQUIV
FREQUENCY COUNTER 2	HEWLETT PACKARD 5345A OR EQUIV (B/A FUNCTION $f_{in} \geq$ 35 MHz FOR INPUTS A & B)
DC POWER SUPPLY	TEKTRONIX PS503A OR EQUIV (4.5-5.5 V, 200 mA)
TEMPERATURE TEST CHAMBER	STATHAM SD6-1
TEMPERATURE MONITOR	DORIC TRENDICATOR 400A TYPE J/°C

Figure 18. SN54/74LS297 AC Performance Test Diagram
Maximum Input Frequency Test – K Clock Input (Pin 4)

TABLE 8. SUMMARY OF MAXIMUM CLOCK INPUT FREQUENCY CHARACTERIZATION DATA (SN54LS297 EVALUATION LOT #419)

SN54LS297 Maximum Clock Input Frequency (f_{max}) – MHz														
Test Temp.	Clock Pin Test I/D Function		I/D CLK INC	I/D CLK DEC	K CLK INC	K CLK DEC	I/D CLK INC	I/D CLK DEC	K CLK INC	K CLK DEC	I/D CLK INC	I/D CLK DEC	K CLK INC	K CLK DEC
			V_{CC} = 4.5 V				V_{CC} = 5.0 V				V_{CC} = 5.5 V			
−55°C	f_{max}	Mean	26.4	24.8	40.0	37.7	31.5	30.9	52.5	51.4	34.8	34.9	58.4	57.7
		Std. Dev.	2.0	2.0	4.4	3.6	2.0	2.0	3.6	4.3	2.1	2.1	2.1	1.9
0°C	f_{max}	Mean	29.9	31.1	52.9	52.2	34.1	35.6	58.5	57.6	37.2	38.7	64.1	62.9
		Std. Dev.	1.1	1.0	1.6	1.6	1.2	1.2	2.6	1.8	1.8	1.5	2.0	2.4
25°C	f_{max}	Mean	30.7	32.4	52.9	52.9	35.1	36.0	56.4	55.8	37.0	38.5	62.1	60.3
		Std. Dev.	1.38	0.84	0.95	0.7	0.5	1.0	0.8	1.0	0.7	1.1	2.4	2.4
70°C	f_{max}	Mean	30.2	30.9	48.3	47.9	33.0	33.8	52.9	51.6	35.1	35.9	54.8	53.6
		Std. Dev.	1.6	1.2	2.0	1.5	1.2	1.1	1.5	1.9	1.5	1.4	0.8	1.1
125°C	f_{max}	Mean	27.1	24.8	39.6	38.9	26.6	23.9	40.6	39.2	22.6	21.1	41.0	38.6
		Std. Dev.	1.3	1.4	1.1	1.2	3.0	3.2	0.8	1.2	3.3	3.6	1.0	1.7

TABLE 9. SN54/74LS297 SWITCHING CHARACTERISTICS

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN (−55°C to 125°C, 4.5 V to 5.5 V)	TYP (25°C, 5.0 V)	MAX	UNITS
f_{max}	Maximum input frequency	K CLK			30	50		MHz
		I/D CLK			15	35		MHz
t_{PLH}	Propagation delay, I/D output low to high	I/D CLK	I/D OUT			15		ns
t_{PHL}	Propagation delay, I/D output high to low	I/D CLK	I/D OUT			22		ns
t_{PLH}	Propagation delay, EXORPD output low to high	ϕ_A or ϕ_B	EXOR OUT	Other input low		10		ns
				Other input high		17		ns
t_{PHL}	Propagation delay, EXORPD output high to low	ϕ_A or ϕ_B	EXOR OUT	Other input low		15		ns
				Other input high		17		ns
t_{PLH}	Propagation delay, ECPD output low to high	ϕ_B	ECPD OUT			20		ns
t_{PHL}	Propagation delay, ECPD output high to low	ϕ_A'	ECPD OUT			20		ns
t_{su}	Set-up time prior to K CLK positive transition	U/D or ENA	K CLK			25		ns
t_h	Hold time, after K CLK positive transition	U/D or ENA	K CLK			0		ns

NOTE: Typical values based on SN54/74LS297 lot 419 data. Final data sheet specification of min and max values to be determined from additional LS297 characterization material.

F. STANDARD SN54LS ENVIRONMENTAL TESTS AND RELIABILITY DATA

As a standard catalog part, the SN54LS297 DPLL will undergo standard military electrical and environmental testing procedures. Table 10 summarizes the screening and lot conformance standards applicable to Texas Instruments MIL-M-38510/MIL-STD-883 Class B devices.

No reliability testing program was required for this DPLL evaluation. A prediction of the SN54/74LS297 reliability can be made from existing Low Power Schottky reliability studies. A sample two-level metal Low Power Schottky device reliability study is presented in Table 11.

G. DPLL PHASE LOCK TEST DATA

Tables 12, 13, 14, and 15 present data from the SN54LS297 phase lock tests conducted on the four DPLL circuit configurations of Figure 2. For the test, the input signal $f_{IN} \angle \phi_{IN}$ was supplied by a Hewlett Packard 3325A frequency synthesizer with microhertz resolution. The output signal $f_{OUT} \angle \phi_{OUT}$ was monitored with similar accuracy using a HP 5345A electronic counter. This equipment was synchronized to the 10.000000000 MHz crystal-controlled clock applied to the K-clock and I/D clock inputs. The external ÷N feedback counter with N=256 set the loop center frequency f_c at 19531.25 kHz. The K-decode inputs were varied to obtain lock data over the entire bandwidth range of the SN54LS297 DPLL ($2^3 \leqslant K \leqslant 2^{17}$).

The data presented in Tables 12 through 15 corresponds to the lock equations given in Section III.

TABLE 10. TEXAS INSTRUMENTS SCREENING AND LOT CONFORMANCE MIL-M-38510/MIL-STD-883–CLASS B

	SNJ JEDEC SCREENING STD.*		SNC MACH-IV	
SCREEN	**METHOD**	**RQMT**	**METHOD**	**RQMT**
Internal Visual (Precap)	2010 Condition B and 38510	100%	2010 Condition B and 38510	100%
Stabilization Bake	1008 24 hours minimum test Condition C	100%	1008 24 hours minimum test Condition C	100%
Temperature Cycling	1010 Condition C	100%	1010 Condition C	100%
Constant Acceleration	2001 Condition E (min.) in Y_1 plane	100%	2001 Condition E (min.) in Y_1 plane	100%
Seal Fine & Gross	1014	100%	1014	100%
Interim Electrical	TI data sheet electrical specifications	As applicable	TI data sheet electrical specifications	As applicable
Burn-In test	1015 Note 3 125°C minimum PDA = 10%	100%	1015.1 125°C minimum PDA = 10%	100%
Final Electrical Tests (a) Static tests (1) 25°C (Subgroup 1, table 1, 5005) (2) Max and min rated op. temperature (subgroups 2 and 3 table 1, 5005) (b) Dynamic tests and switching tests 25°C (subgroup 4 and 9 table 1, 5005) (c) Functional test 25°C (subgroup 7, table 1, 5005)	TI data sheet electrical specifications	100% 100% 100% 100% Note 4	TI data sheet electrical specifications	100% 100% Note 1 100%
Quality conformance inspection Group A (a) Static (1) 25°C (Subgroup 1) (2) Temp. (Subgroup 2 & 3) (b) Switching (1) 25°C (Subgroup 9) (2) Temp. (Subgroup (10 & 11) (c) Functional (1) 25°C (Subgroup 7)	5005 Class B Note 3	Note 2 LTPD 3% 5% 5% 3%	5005 Class B	Note 2 LTPD 3% 5% 5% 3%
Group B	5005 Class B	6 weeks package prod.	5005 Class B	6 weeks package prod.
Group C	5005 Class B	13 weeks prod.	5005 Class B	13 weeks prod.
Group D	5005 Class B	6 months package prod.	5005 Class B	6 months package prod.
External Visual	2009	100%	2009.1	100%

*Per JEDEC Publication 101 Screening Standard.

NOTE 1 Temperature guardband test may be used in lieu of 100% test for digital bipolar only
NOTE 2 Group A per 5005 Generic data available for groups B, C and D per CB-159
NOTE 3 Includes group A report.
NOTE 4 100% functionally tested at temperature extremes

TABLE 11. LOW POWER SCHOTTKY RELIABILITY DATA

Device Tested	SN74LS245N, SN74LS647N (2-Level Metal Devices)	Regular Production Low Power Schottky Devices
Samples	156	4276
Failures	2	38
Total Device Hours at 125°C	156,000	6,546,000
Equivalent Device Hours at 55°C Based on 0.96 eV Activation Energy	6.13×10^7	2.57×10^9
125°C Failure Rate/1 K hours	1.28%	0.58%
55° Failure Rate/1 K hours at a 60% upper confidence level	0.0051%	0.0016%
Mean Time Between Failure	30×10^6	67×10^6

The parameter Q increases with increasing K or decreasing bandwidth according to Eq. (9). The measured output jitter or phase resolution is 1/2N cycles or 0.7 degrees referenced to f_c. Resolution of the Δf input frequency deviation increased with K according to Eq. (6) and the phase resolution.

As discussed in Section III the theoretical phase error limit for the Exclusive-OR phase detector is ±0.25 cycles or ±90°. For the Edge Controlled phase detector, the $\phi_{E\ max}$ is theoretically ±0.5 cycles or ±180°. For the two loop test circuits without ripple cancellation (Tables 12 and 13), the $\phi_{E\ max}$ phase error lock range was equal to the theoretical phase detector phase tracking limits reduced by the factors of the 0.7° phase resolution and the phase detector propagation delays given in Table 9.

For the two circuits with ripple cancellation (Tables 14 and 15), it was determined that the maximum phase error $\phi_{E\ max}$ for the locked condition was reduced by a factor $(1+1/2K)^{-1}$. Omitting factors of phase resolution and phase detector propagation delay, the theoretical phase error limit for the EXORPD ripple cancellation circuit of Figure 2(c) was derived to be:

$$\phi_{E\ max} = \frac{0.25}{1+1/2K} \quad \text{cycles} \tag{12}$$

Similarly for the ECPD ripple cancellation circuit [Figure 2(d)]:

$$\phi_{E\ max} = \frac{0.5}{1+1/2K} \quad \text{cycles} \tag{13}$$

For these ripple cancellation circuits, the Eq. (5) lock range relationship is modified by the above limits on phase error ϕ_E and by a 50% reduction in phase detector gain K_D. For the ripple cancellation circuits of Figures 2(c) and 2(d), the theoretical lock range becomes:

$$\Delta f_{max} = f_{OUT\ max} - f_c = \left(\frac{1}{1+1/2K}\right)\frac{Mf_c}{4KN} \quad H_Z \tag{14}$$

TABLE 12. SN54LS297 PHASE LOCK TEST DATA – EXOR PHASE DETECTOR DPLL CIRCUIT [FIGURE 2(a)] (M = 2N - 512; f_c = 19531.25 Hz; K CLOCK, I/D CLOCK f_{IN} = 10 MHz)

K	Q $\left(\frac{\pi K}{K_D}\right)$	ϕ_E Phase Error Resolution (1/2N) (degrees)	Δf Frequency Resolution (Hz)	$\phi_{E\ max}$ Phase Error Lock Range (degrees)	Δf_{max} $f_{IN} - f_c$ Frequency Lock Range (Hz)	$f_{OUT\ max}$ Maximum Lock Frequency (Hz)	$f_{OUT\ min}$ Minimum Lock Frequency (Hz)	Ripple (Phase Error in ÷N Counter) $f_{IN} = f_c$ (cycles)
2^3	6.3	±0.70	19.07	90 ± 89.3	2422.33276	21953.58276	17108.91724	8/N
2^5	25.1	±0.70	4.76	90 ± 89.3	605.58319	20136.83319	18925.66681	2/N
2^7	100.5	±0.70	1.19	90 ± 89.3	151.39579	19682.64580	19379.85420	1/N
2^9	402.1	±0.70	2.98×10^{-1}	90 ± 89.3	37.84894	19569.09895	19493.40105	1/N
2^{11}	1608.5	±0.70	7.45×10^{-2}	90 ± 89.3	9.46223	19540.71224	19521.78776	1/N
2^{13}	6434	±0.70	1.86×10^{-2}	90 ± 89.3	2.36555	19533.61556	19528.88444	1/N
2^{15}	25736	±0.70	4.65×10^{-3}	90 ± 89.3	0.59138	19531.84139	19530.65861	1/N
2^{17}	102944	±0.70	1.16×10^{-3}	90 ± 89.3	0.14784	19531.39785	19531.10215	1/N

TABLE 13. SN54LS297 PHASE LOCK TEST DATA – EDGE CONTROLLED PHASE DETECTOR DPLL CIRCUIT [FIGURE 2(b)] (M = N = 512; f_c 19531.25 Hz; K CLOCK, I/D CLOCK f_{IN} = 10 MHz)

K	Q $\left(\frac{\pi K}{K_D}\right)$	ϕ_E Phase Error Resolution (1/2N) (degrees)	Δf Frequency Resolution (Hz)	$\phi_{E\ max}$ Phase Error Lock Range (degrees)	Δf_{max} $f_{IN} - f_c$ Frequency Lock Range (Hz)	$f_{OUT\ max}$ Maximum Lock Frequency (Hz)	$f_{OUT\ min}$ Minimum Lock Frequency (Hz)	Ripple (Phase Error in ÷N Counter) $f_{IN} = f_c$ (cycles)
2^3	12.6	±0.70	9.53	180 ± 177.9	2412.79602	21953.58276	17118.45398	16/N
2^5	50.3	±0.70	2.38	180 ± 177.9	603.19900	20136.83319	18928.05099	4/N
2^7	201.1	±0.70	5.96×10^{-1}	180 ± 177.9	150.79975	19682.64580	19380.45025	1/N
2^9	804.2	±0.70	1.49×10^{-1}	180 ± 177.9	37.69993	19569.09895	19493.55006	1/N
2^{11}	3217	±0.70	3.72×10^{-2}	180 ± 177.9	9.42498	19540.71224	19521.82502	1/N
2^{13}	12868	±0.70	9.31×10^{-3}	180 ± 177.9	2.35624	19533.61556	19528.89375	1/N
2^{15}	51472	±0.70	2.32×10^{-3}	180 ± 177.9	0.58906	19531.84139	19530.66094	1/N
2^{17}	205887	±0.70	5.82×10^{-3}	180 ± 177.9	0.14726	19531.39785	19531.10273	1/N

TABLE 14. SN54LS297 PHASE LOCK TEST DATA – EXOR RIPPLE CANCELLATION DPLL CIRCUIT [FIGURE 2(c)] (M = N = 512; f_c 19531.25 Hz; K CLOCK, I/D CLOCK f_{IN} = 10 MHz)

K	Q $\left(\frac{\pi K}{K_D}\right)$	ϕ_E Phase Error Resolution (1/2N) (degrees)	Δf Frequency Resolution (Hz)	$\phi_{E\,max}$ Phase Error Lock Range (degrees)	Δf_{max} $f_{IN} - f_c$ Frequency Lock Range (Hz)	$f_{OUT\,max}$ Maximum Lock Frequency (Hz)	$f_{OUT\,min}$ Minimum Lock Frequency (Hz)	Ripple (Phase Error in ÷N Counter) $f_{IN} = f_c$ (cycles)
2^3	12.6	±0.70	9.53	0 ± 84.0	1139.36031	20670.61032	18320.08362	1/N
2^5	50.3	±0.70	2.38	0 ± 87.9	298.09658	19829.34658	19228.45840	1/N
2^7	201.1	±0.70	5.96×10^{-1}	0 ± 88.9	75.40103	19606.65110	19455.55210	1/N
2^9	804.2	±0.70	1.49×10^{-1}	0 ± 89.3	18.92447	19550.17447	19512.32553	1/N
2^{11}	3217	±0.70	3.72×10^{-2}	0 ± 89.3	4.73111	19535.98112	19526.51888	1/N
2^{13}	12868	±0.70	9.31×10^{-3}	0 ± 89.3	1.18277	19532.43278	19530.06722	1/N
2^{15}	51472	±0.70	2.32×10^{-3}	0 ± 89.3	0.29569	19531.54569	19530.95431	1/N
2^{17}	205887	±0.70	5.82×10^{-3}	0 ± 89.3	0.07923	19531.32392	19531.17608	1/N

TABLE 15. SN54LS297 PHASE LOCK TEST DATA – EDGE CONTROLLED RIPPLE CANCELLATION DPLL CIRCUIT [FIGURE 2(d)] (M = N = 512; f_c 19531.25 Hz; K CLOCK, I/D CLOCK f_{IN} = 10 MHz)

K	Q $\left(\frac{\pi K}{K_D}\right)$	ϕ_E Phase Error Resolution (1/2N) (degrees)	Δf Frequency Resolution (Hz)	$\phi_{E\,max}$ Phase Error Lock Range (degrees)	Δf_{max} $f_{IN} - f_c$ Frequency Lock Range (Hz)	$f_{OUT\,max}$ Maximum Lock Frequency (Hz)	$f_{OUT\,min}$ Minimum Lock Frequency (Hz)	Ripple (Phase Error in ÷N Counter) $f_{IN} = f_c$ (cycles)
2^3	25.1	±0.70	4.76	180 ± 168.0	1139.36031	20670.61032	18320.08362	1/N
2^5	100.5	±0.70	1.19	180 ± 175.9	298.09658	19829.34658	19228.45840	1/N
2^7	402.1	±0.70	2.9×10^{-1}	180 ± 177.9	75.40103	19606.65110	19455.55210	1/N
2^9	1608.5	±0.70	7.4×10^{-2}	180 ± 178.6	18.92447	19550.17447	19512.32553	1/N
2^{11}	6434	±0.70	1.8×10^{-2}	180 ± 178.6	4.73111	19535.98112	19526.51888	1/N
2^{13}	25736	±0.70	4.6×10^{-3}	180 ± 178.6	1.18277	19532.43278	19530.06722	1/N
2^{15}	102944	±0.70	1.2×10^{-3}	180 ± 178.6	0.29569	19531.54569	19530.95431	1/N
2^{17}	411774	±0.70	2.9×10^{-4}	180 ± 178.6	0.07923	19531.32392	19531.17608	1/N

The $f_{OUT\ max}$ and $f_{OUT\ min}$ lock range data presented in Tables 12 through 15 corresponds to the predicted lock range calculated from Eqs. (5) and (14) when adjusted for limits imposed by phase resolution and phase detector propagation delay.

The phase lock data demonstrates the dynamic range available with the programmable bandwidth of the DPLL. For example, the standard EXORPD DPLL circuit (Table 12) had a bandwidth that varied from ±2200 Hz to ±0.14 Hz. The ripple cancellation circuits offered the highest frequency resolution and effectively reduced ripple in the ÷N feedback counter. For minimum ripple and optimum performance of all four DPLL circuits, particular attention must be paid to the set-up and hold requirements of the U/D and ENA inputs (Table 9).

SECTION VII
RESULTS AND CONCLUSIONS

The SN54LS297 Digital Phase-Locked Loop evaluation devices successfully met all dc and ac performance specifications of the contract. Empirical phase-lock data agreed with theoretically predicted performance. Maximum operating speed meets the approved design goals and requirements presented at the 1 August 1979 DPLL design review with AFAL. Device performance, yield, and reliability should meet Low Power Schottky requirements for introduction as a standard LS catalog part for both commercial and military markets.

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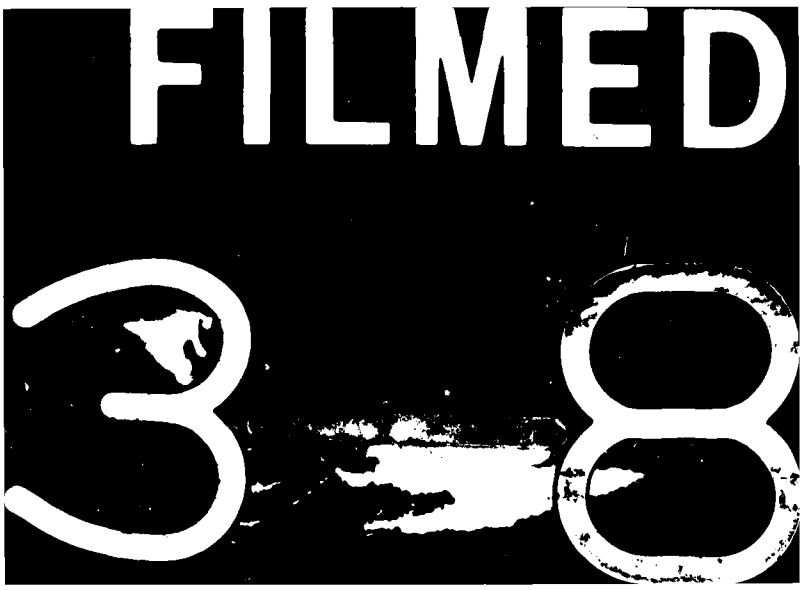
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